★ Super Low Gate Charge
★ Green Device Available
★ Excellent CdV/dt effect decline
★ Advanced high cell density Trench technology

Product Summary

Green

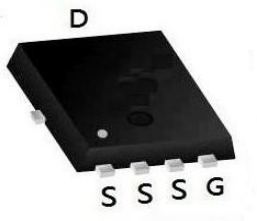
BVDSS	RDSON	ID
-20V	2.2mΩ	-120A

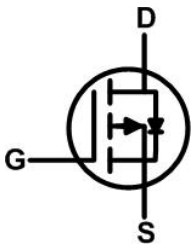
Description

The XR120P02F is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The XR120P02F meet the RoHS and Green Product requirement with full function reliability approved.

PDFN5060-8L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	±12	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	-120	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	-60	A
I_{DM}	Pulsed Drain Current[2]	-480	A
EAS	Single Pulse Avalanche Energy[3]	155	mJ
I_{AS}	Avalanche Current	25	A
P_D@T_C=25℃	Total Power Dissipation[4]	124	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	4.4	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	1.1	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	---	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V , I_D=-30A	---	2.2	2.9	mΩ
		V_{GS}=-2.5V , I_D=-20A	---	3	4	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.55	-0.75	-1	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-20V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-20V, V_{GS}=0V , T_J=100℃	---	---	---	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-16A	---	---	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	5.1	---	Ω
Q_g	Total Gate Charge	V_{DS}=-10V , V_{GS}=0 to -10V , I_D=-30A	---	98	---	nC
Q_{gs}	Gate-Source Charge		---	20	---	
Q_{gd}	Gate-Drain Charge		---	25	---	
$T_{d(on)}$	Turn-On Delay Time	V_{GS}=-10V, V_{DS}=-10V, I_D=-30A, R_{GEN}=3Ω	---	19	---	ns
T_r	Rise Time		---	55	---	
$T_{d(off)}$	Turn-Off Delay Time		---	258	---	
T_f	Fall Time		---	138	---	
C_{iss}	Input Capacitance	V_{DS}=-10V , V_{GS}=0V , f=1MHz	---	10611	---	pF
C_{oss}	Output Capacitance		---	1368	---	
C_{rss}	Reverse Transfer Capacitance		---	901	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-120	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-11A , T_J=25℃	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	IF=-30A , di/dt=100A/μs , T_J= 25℃	---	38	---	nS
Q_{rr}	Reverse Recovery Charge		---	29	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is TJ = 25℃,VDD=-16V,VGS=-4.5V,L=0.5mH.
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics

Figure 5: Output Characteristics

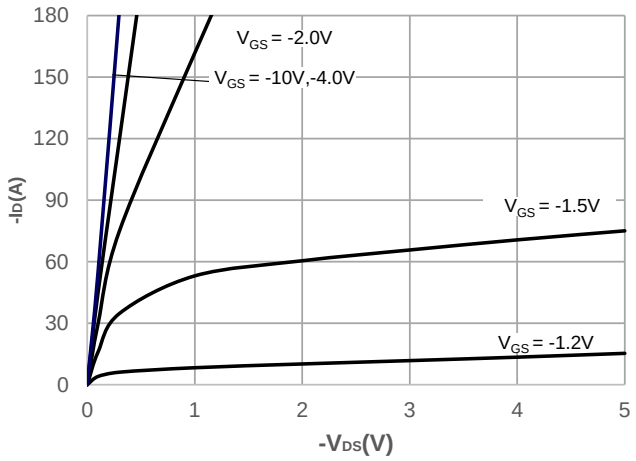


Figure 6: Typical Transfer Characteristics

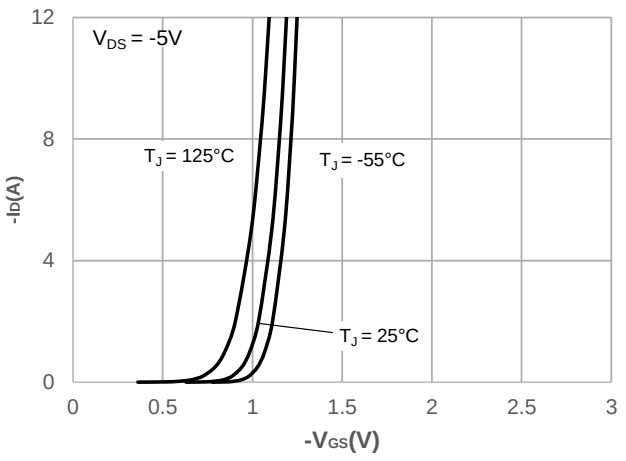


Figure 7: On-resistance vs. Drain Current

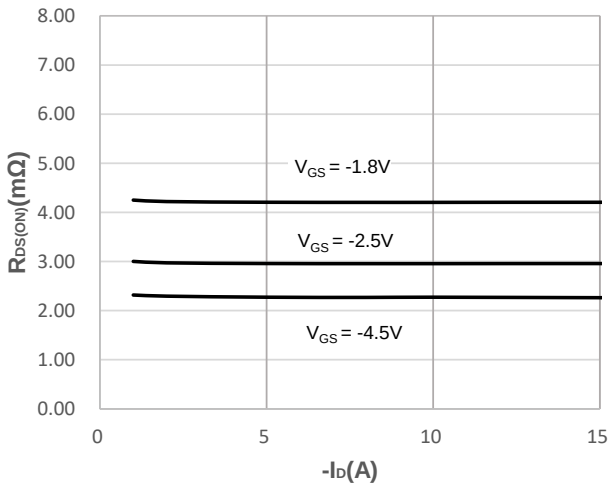


Figure 8: Body Diode Characteristics

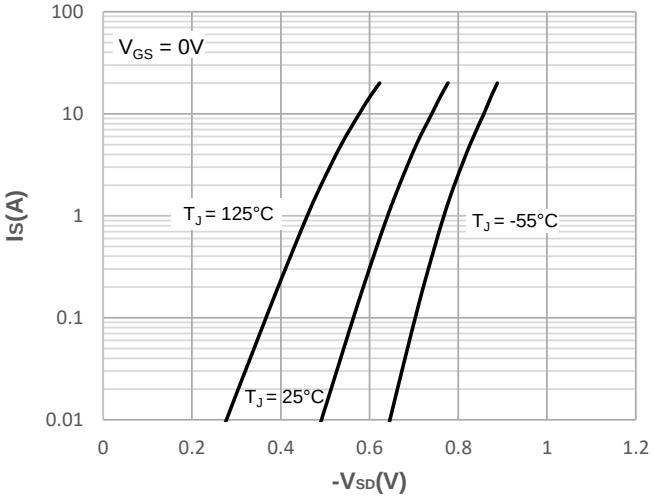


Figure 9: Gate Charge Characteristics

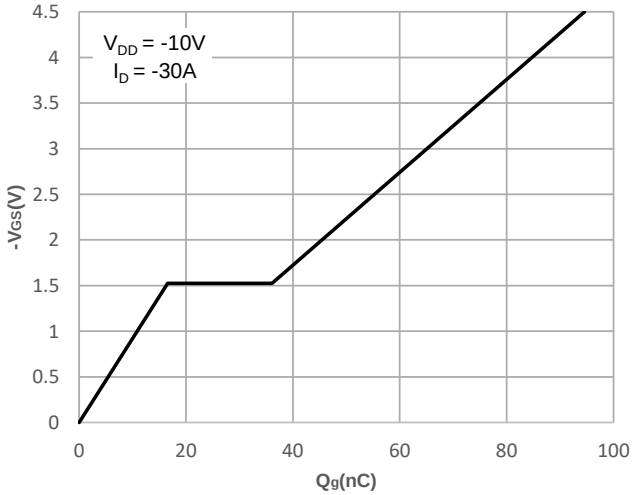


Figure 10: Capacitance Characteristics

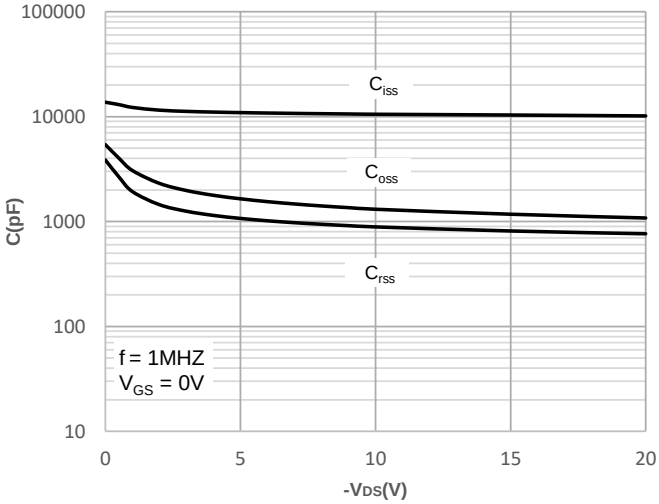


Figure 11: Normalized Breakdown voltage vs. Junction Temperature

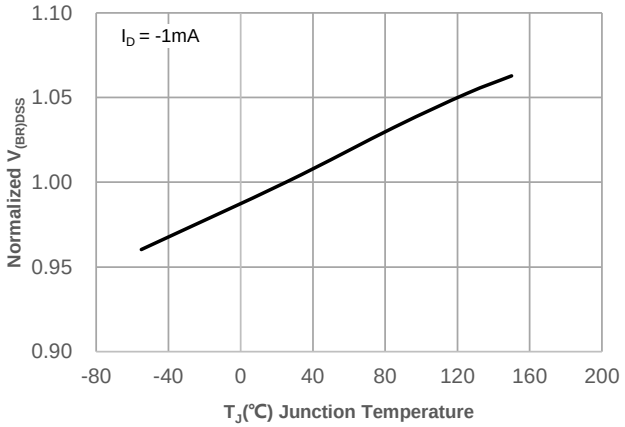


Figure 12: Normalized on Resistance vs. Junction Temperature

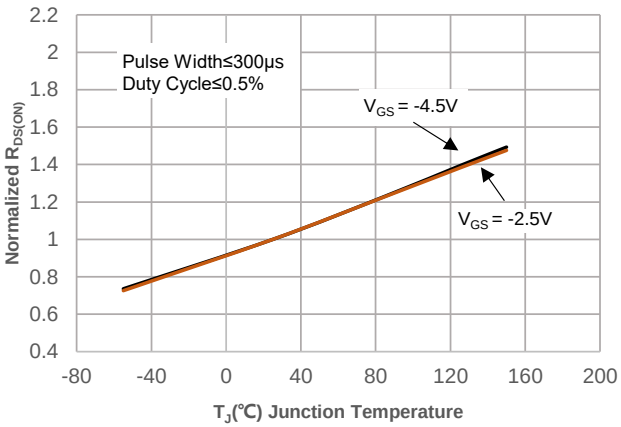


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

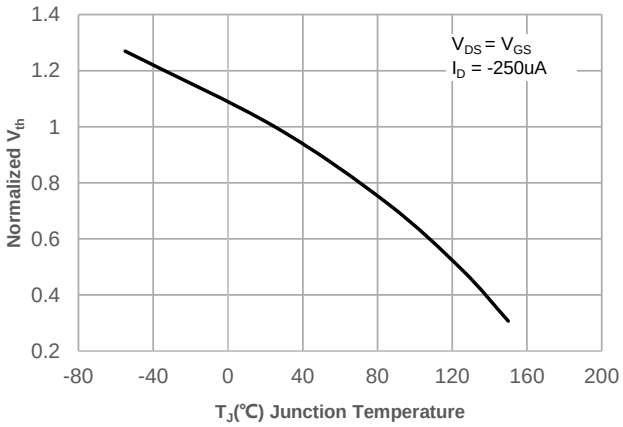


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

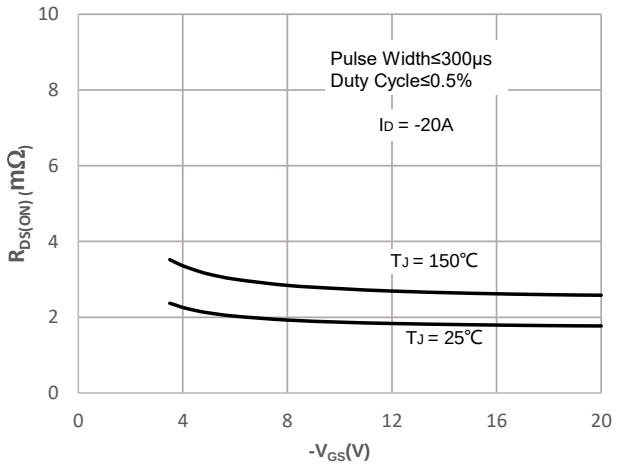


Figure 15: Maximum Safe Operating Area

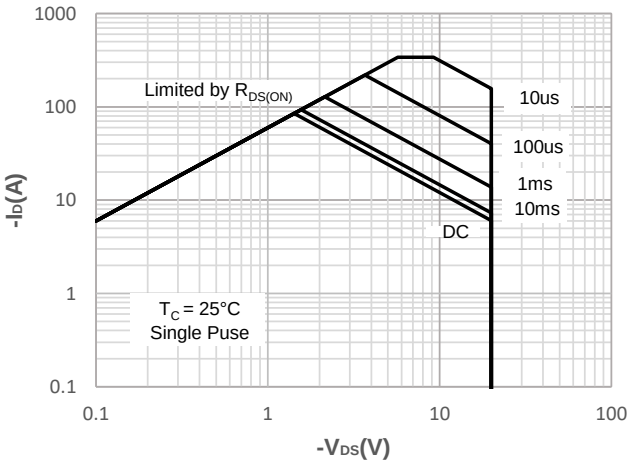


Figure 1: Power De-rating

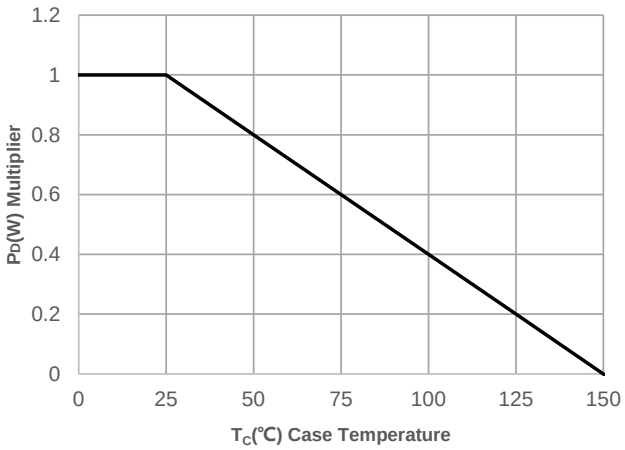


Figure 2: Current De-rating

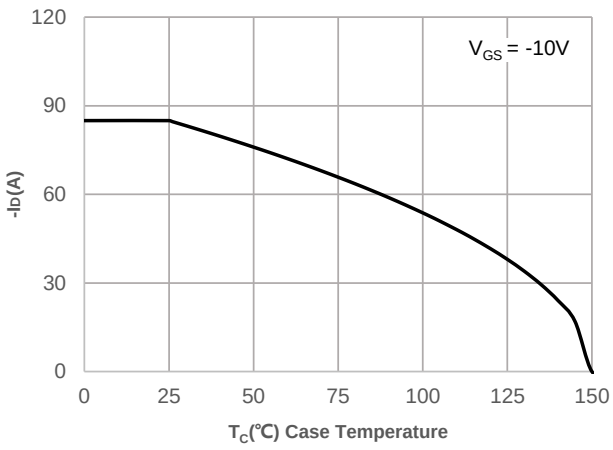


Figure 3: Normalized Maximum Transient Thermal Impedance

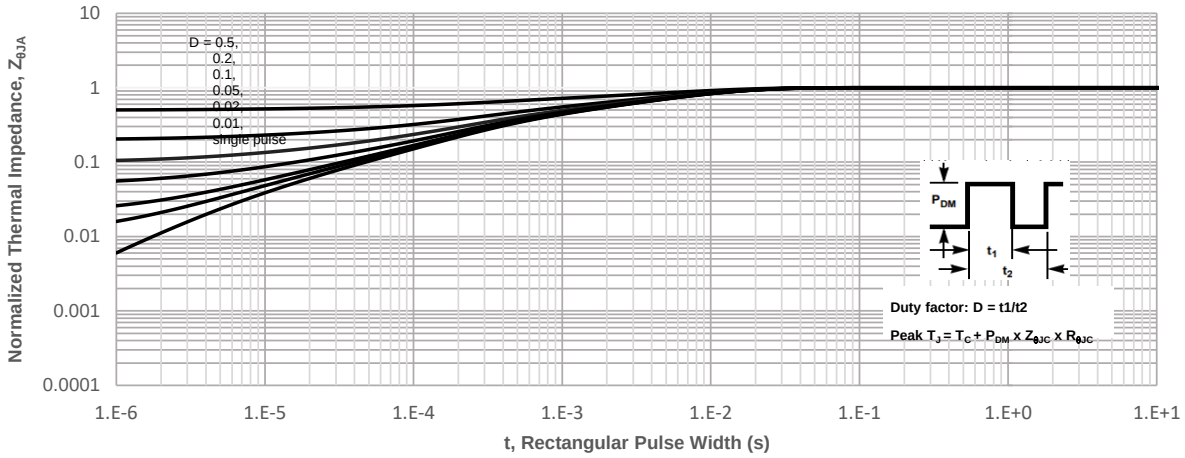
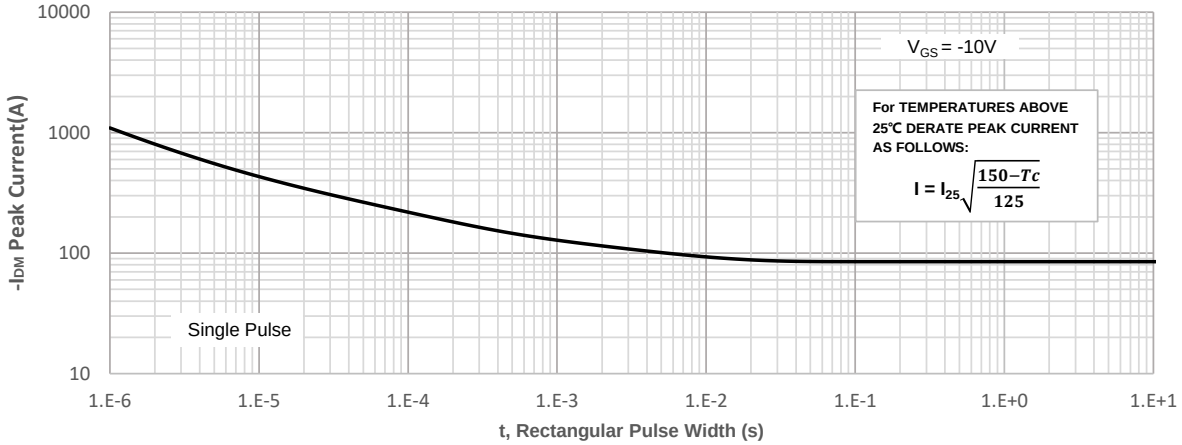


Figure 4: Peak Current Capacity



Test Circuit

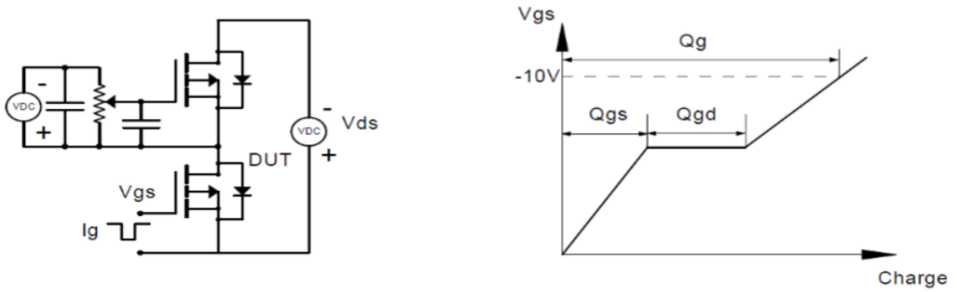


Figure 1: Gate Charge Test Circuit & Waveform

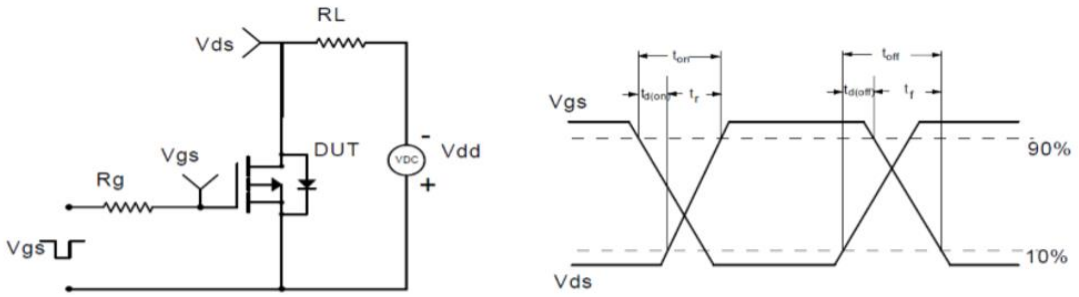


Figure 2: Resistive Switching Test Circuit & Waveform

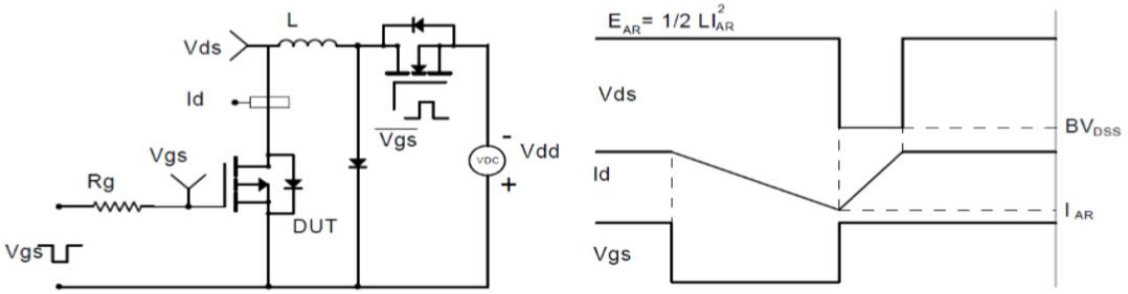


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

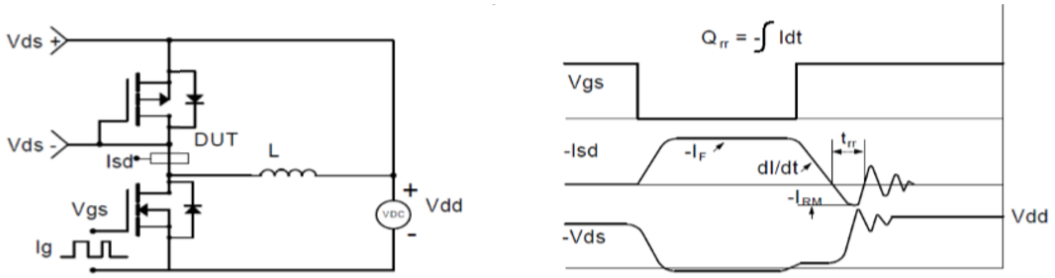
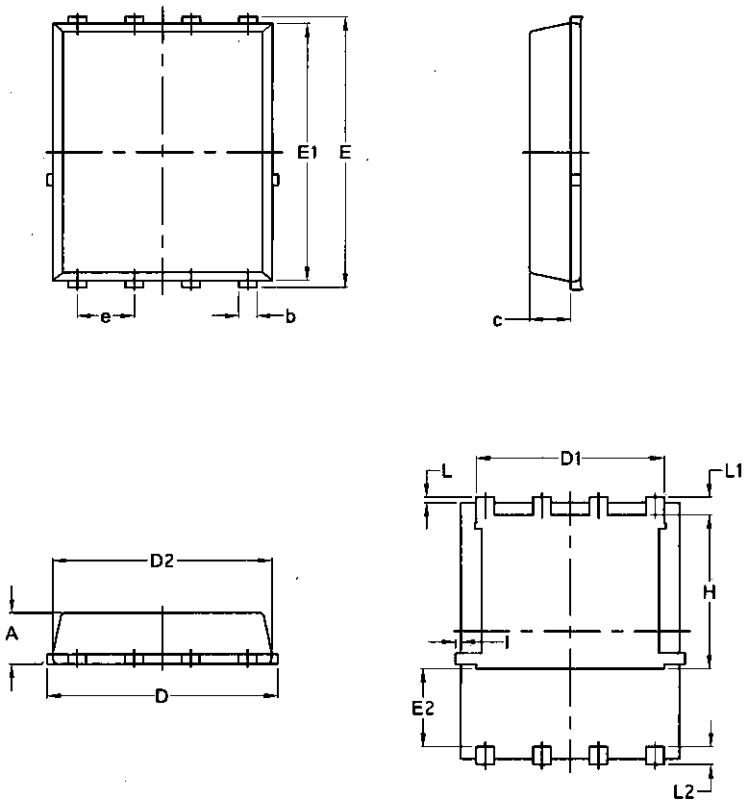


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data-PDFN5060-8L-Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070