

Dual P-Ch 30V Fast Switching MOSFETs

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology



Product Summary

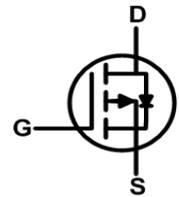
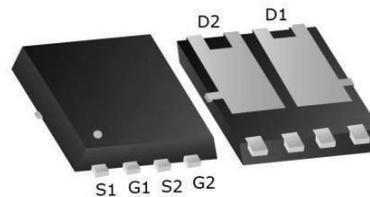
BVDSS	RDSON	ID
-30V	7.2mΩ	-60A

Description

The XR60K03F is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The XR60K03F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PDFN5060-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	-60	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	-35	A
I_{DM}	Pulsed Drain Current ²	-168	A
EAS	Single Pulse Avalanche Energy ³	45	mJ
I_{AS}	Avalanche Current	-30	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	45	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	65	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3.36	$^\circ C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	---	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-1A	---	7.2	11	mΩ
		V _{GS} =-4.5V, I _D =-1A	---	10	18	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1	-1.6	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-30V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-30V, V _{GS} =0V, T _J =100°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-30A	---	57	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	10.5	---	Ω
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-30A	---	30	---	nC
Q _{gs}	Gate-Source Charge		---	5	---	
Q _{gd}	Gate-Drain Charge		---	7.5	---	
T _{d(on)}	Turn-On Delay Time	V _{GS} =-10V, V _{DS} =-15V, I _D = -30A, R _{GEN} =2.5Ω	---	14.1	---	ns
T _r	Rise Time		---	20	---	
T _{d(off)}	Turn-Off Delay Time		---	94	---	
T _f	Fall Time		---	65	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	2396	---	pF
C _{oss}	Output Capacitance		---	325	---	
C _{rss}	Reverse Transfer Capacitance		---	283	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _s	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-60	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-30A, T _J =25C	---	---	-1.2	V

Note :

1. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.1mH, I_{AS}= -30A.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

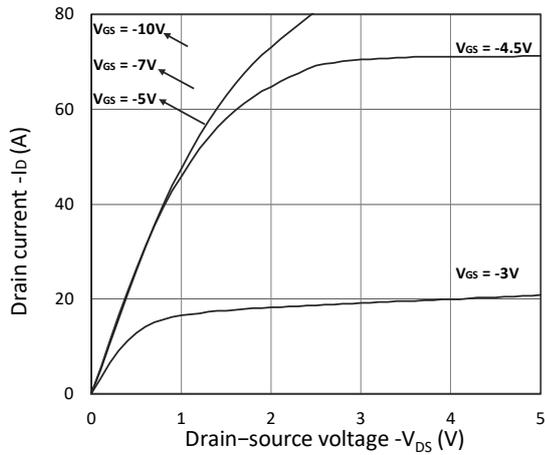


Figure 1. Output Characteristics

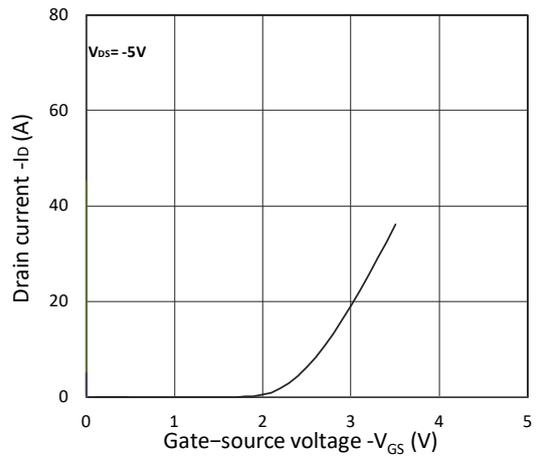


Figure 2. Transfer Characteristics

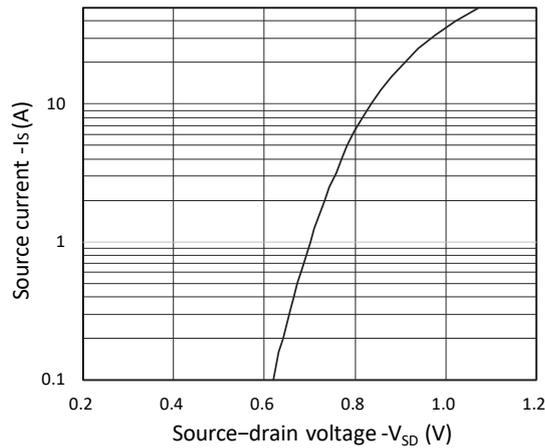


Figure 3. Forward Characteristics of Reverse

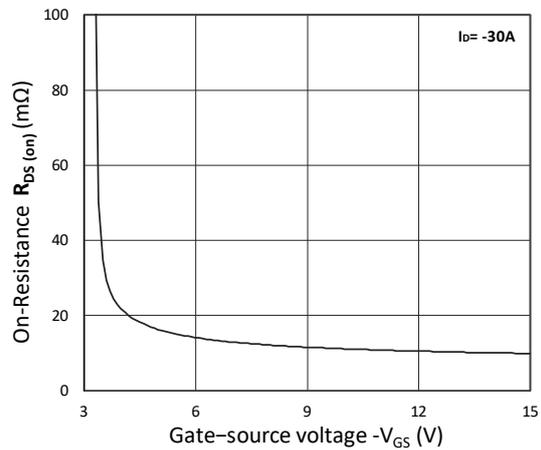


Figure 4. $R_{DS(on)}$ vs. V_{GS}

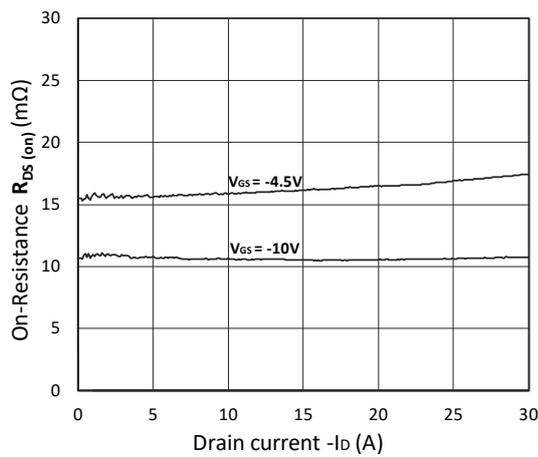


Figure 5. $R_{DS(on)}$ vs. I_D

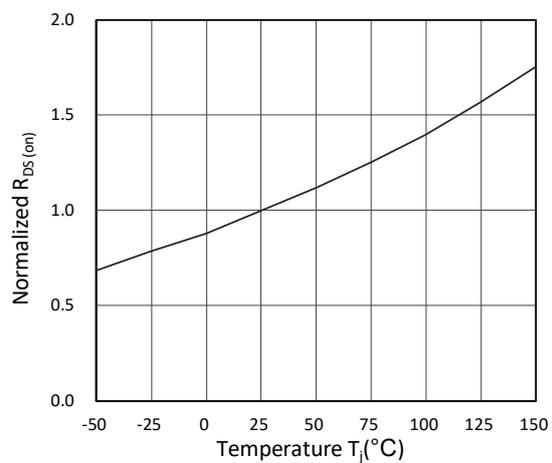


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

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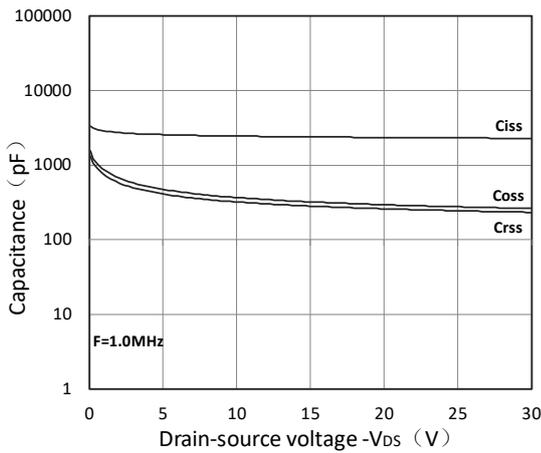


Figure 7. Capacitance Characteristics

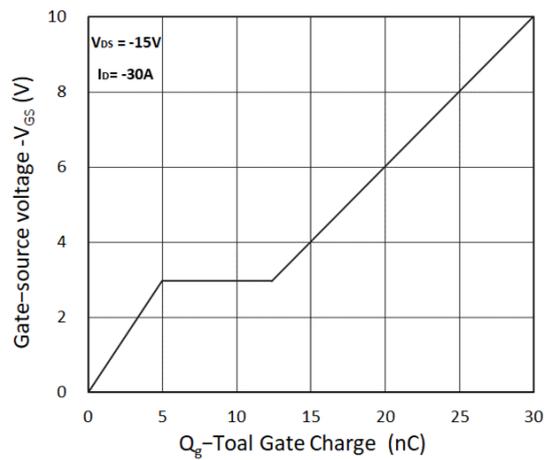


Figure 8. Gate Charge Characteristics

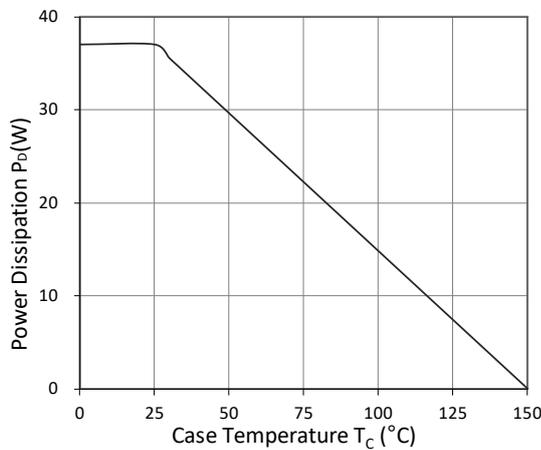


Figure 9. Power Dissipation

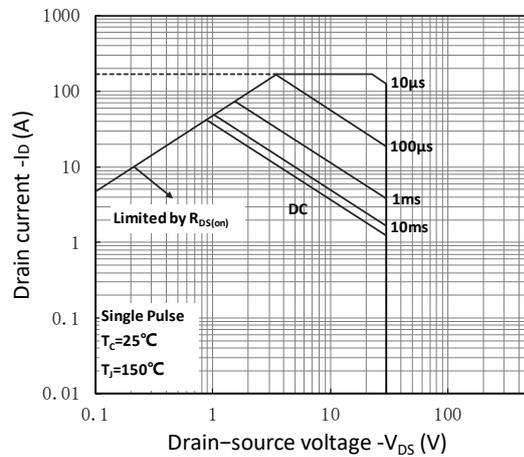


Figure 10. Safe Operating Area

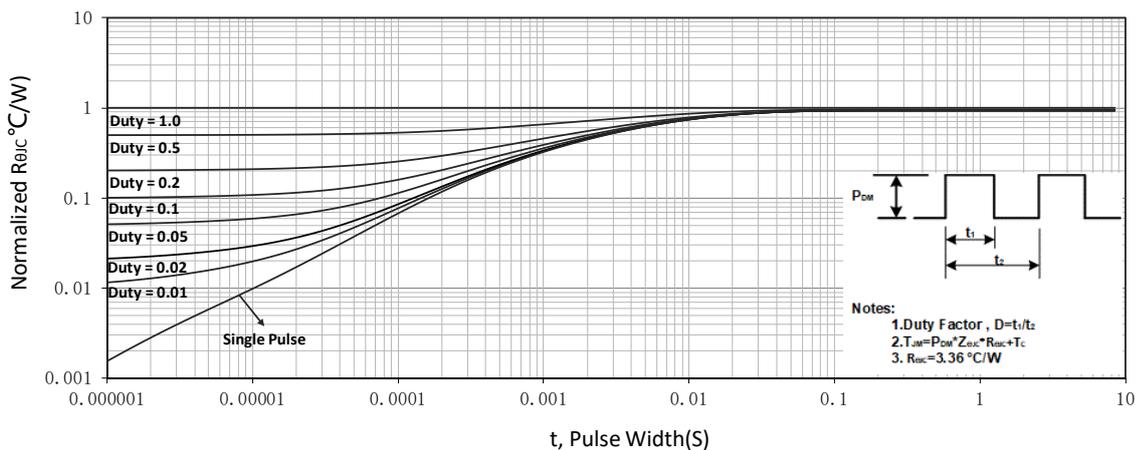
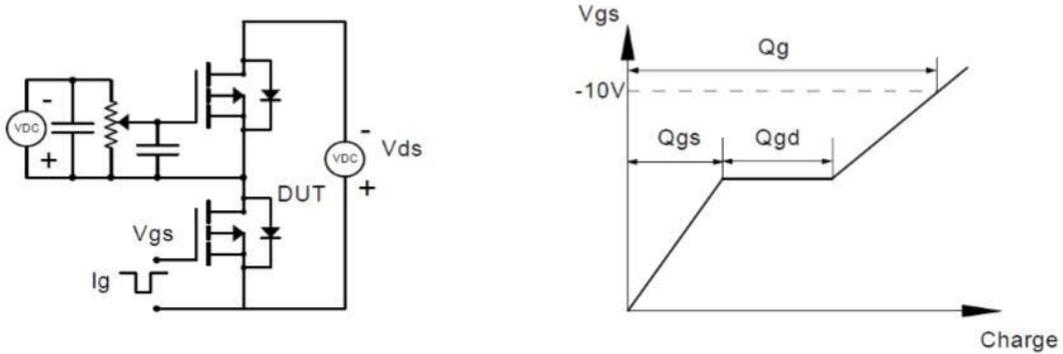


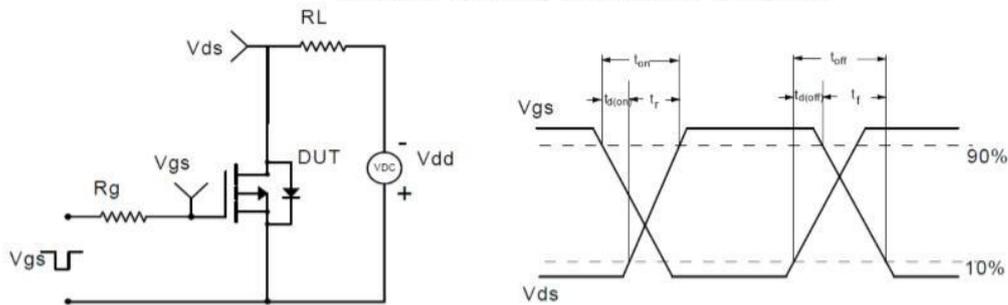
Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

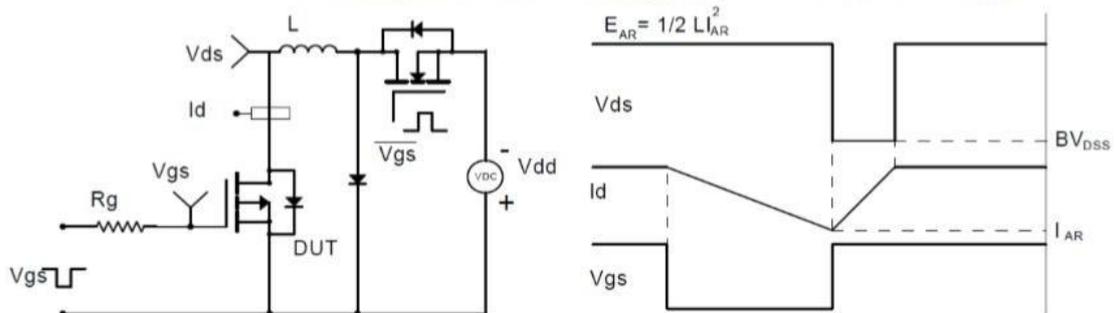
Gate Charge Test Circuit & Waveform



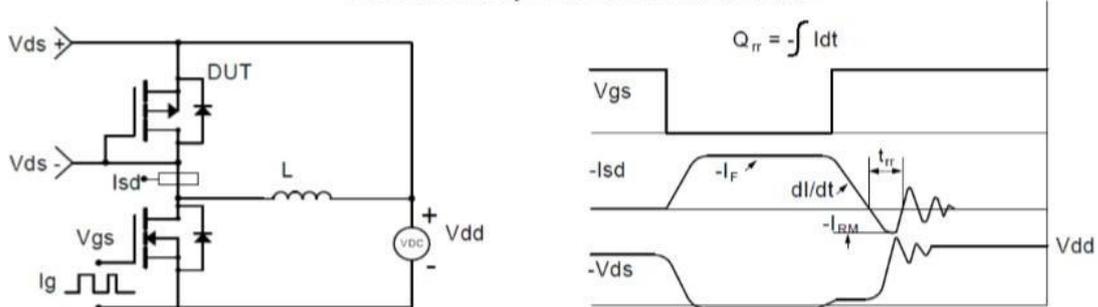
Resistive Switching Test Circuit & Waveforms



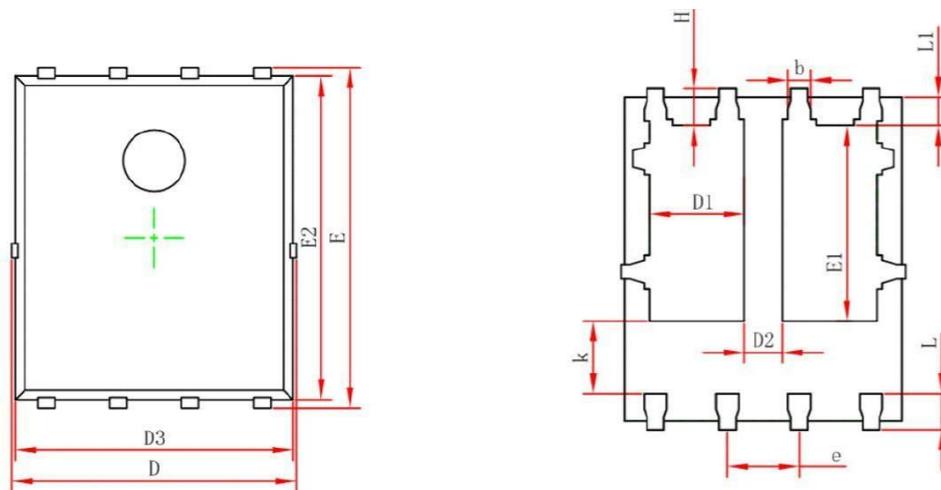
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

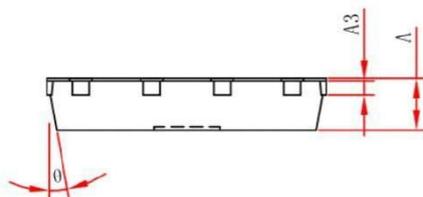


Package Mechanical Data- PDFN5060-8L



Top View

Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.154REF.		0.006REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	1.470	1.870	0.058	0.074
D2	0.470	0.870	0.019	0.034
E1	3.375	3.575	0.133	0.141
D3	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°