P-Ch 20V Fast Switching MOSFETs

★ Super Low Gate Charge
★ Green Device Available
★ Excellent CdV/dt effect decline
★ Advanced high cell density Trench technology

Product Summary

Green

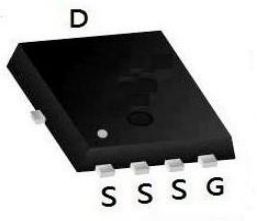
BVDSS	RDSON	ID
-20V	4.5mΩ	65A

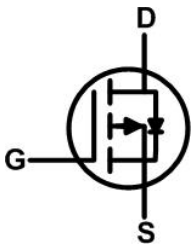
Description

The XR65P02D is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The XR65P02D meet the RoHS and Green Product requirement with full function reliability approved.

PDFN3333-8L Pin Configuration





Absolute (T_j= 25℃ unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	-20	V
I_D	Continuous Drain Current T_C = 25 ℃ (Silicon limited)	-65	A
	Continuous Drain Current T_C = 25 ℃ (Package limited)[a1]	-40	A
	Continuous Drain Current T_C = 100 ℃ (Package limited)[a1]	-40	A
I_{DM}[a1]	Pulsed Drain Current T_C = 25 ℃	-200	A
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}[a2]	Avalanche Energy	98	mJ
P_D	Power Dissipation T_C = 25 ℃	41.6	W
	Derating Factor above 25℃	0.33	W/℃
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	3.0	℃/W
$R_{\theta JA}$	Junction-to-Ambient	64	℃/W

Electrical Characteristics（T_j= 25℃ unless otherwise specified）：

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} =-20V, V_{GS}= 0V, Tj = 25℃	--	--	-1	μA
		V_{DS} =-16V, V_{GS}= 0V, Tj = 125℃	--	--	-100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=10V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-10V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=-4.5V,I_D=-19A	--	4.5	5.6	mΩ
		V_{GS}=-2.5V,I_D=-19A	--	5.9	7.6	mΩ
		V_{GS}=-1.8V,I_D=-19A	--	8.3	11	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D =- 250μA	-0.4	-0.7	-1.0	V
Pulse width tp≤300μs,δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	--	6.3	--	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} =-10V f = 1.0MHz	--	6199	--	pF
C_{oss}	Output Capacitance		--	885.6	--	
C_{rss}	Reverse Transfer Capacitance		--	976	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	T_C = 25 ℃	--	--	-65	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	-200	A
V_{SD}	Diode Forward Voltage	I_S=-19A,V_{GS}=0V	--	--	-1.2	V
Pulse width tp≤300μs,δ≤2%						

[a1]: Calculated continuous current based on maximum allowable junction temperature. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

[a2]: L=0.5mH,Ias=19.8A Start T_J=25℃

[a3]: Recommend soldering temperature defined by IPC/JEDEC J-STD 020

Typical Performance Characteristics

Figure1: Output Characteristics

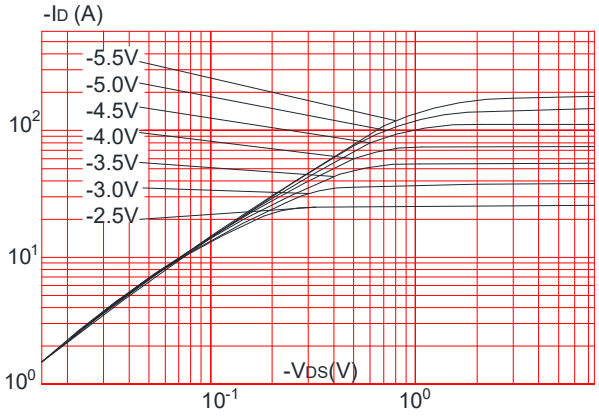


Figure 2: Typical Transfer Characteristics

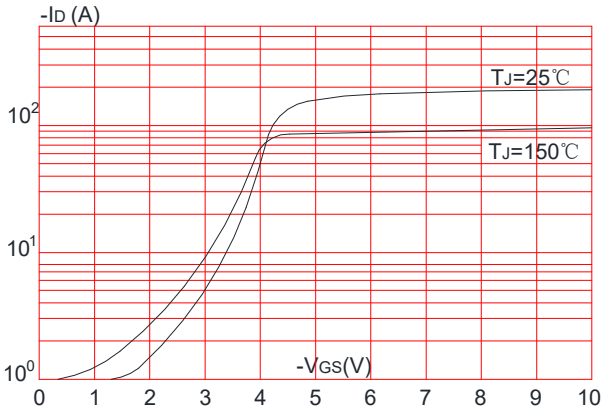


Figure 3: On-resistance vs. Drain Current

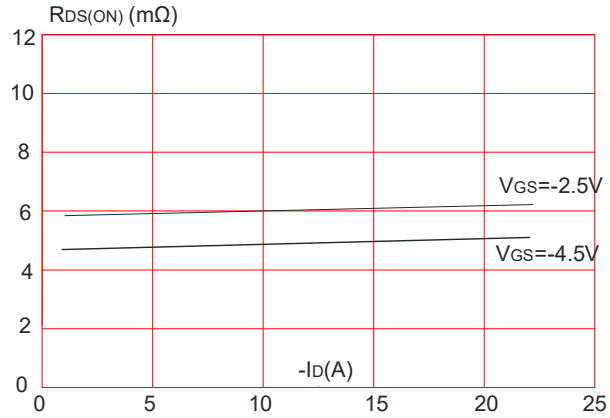


Figure 4: Body Diode Characteristics

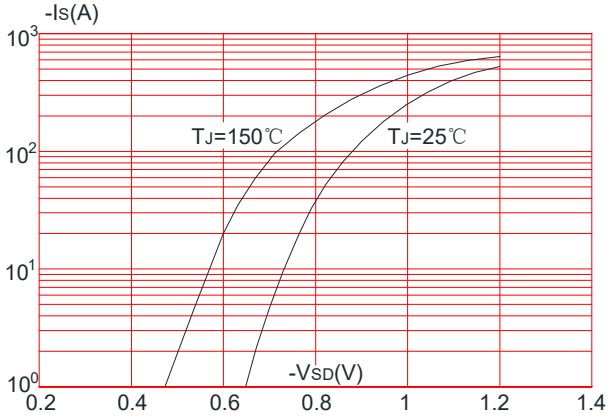


Figure 5: Gate Charge Characteristics

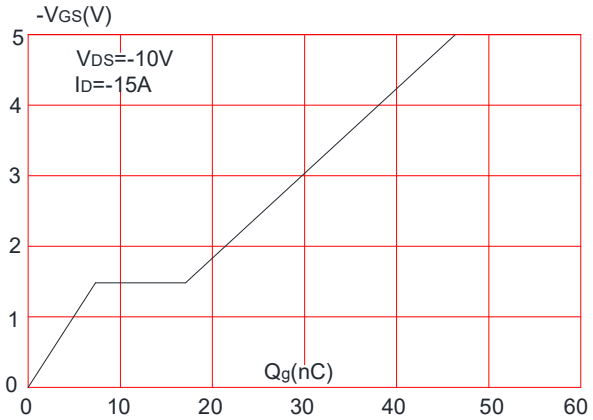


Figure 6: Capacitance Characteristics

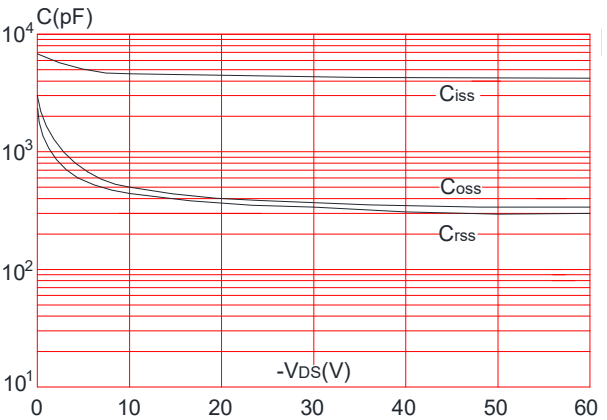


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

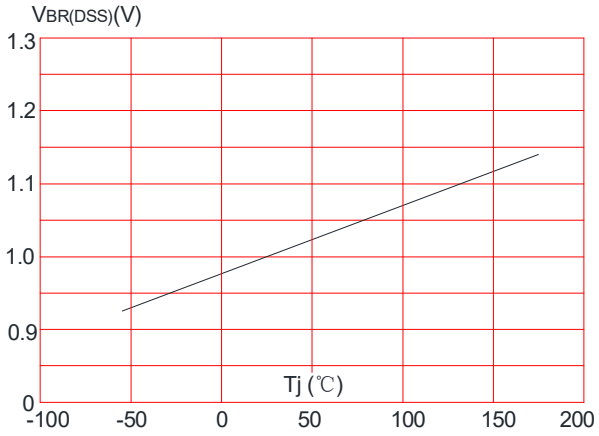


Figure 8: Normalized on Resistance vs. Junction Temperature

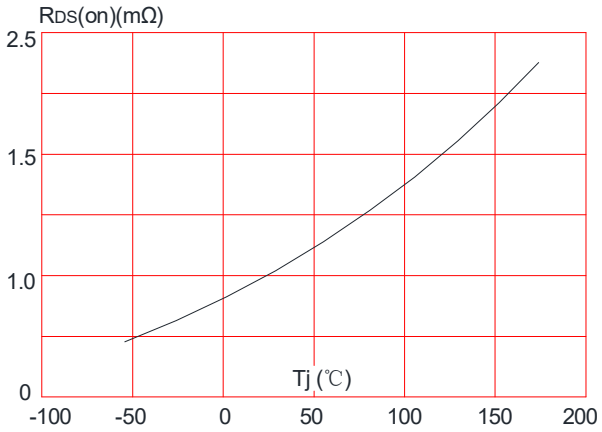


Figure 9: Maximum Safe Operating Area

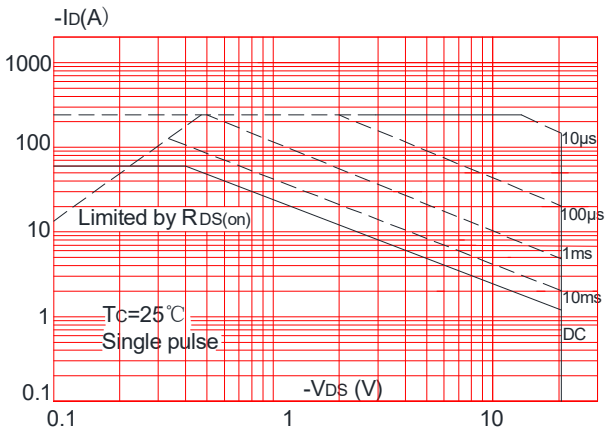


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

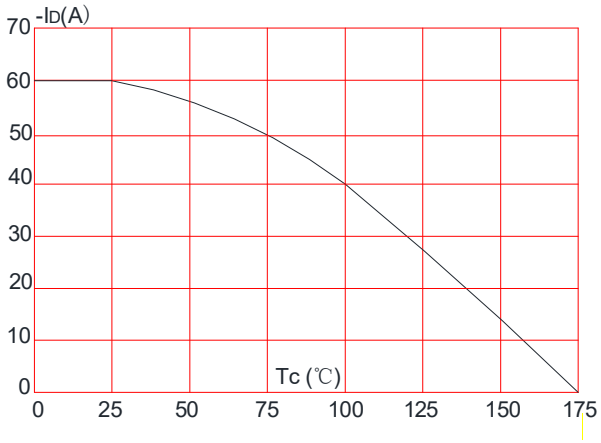
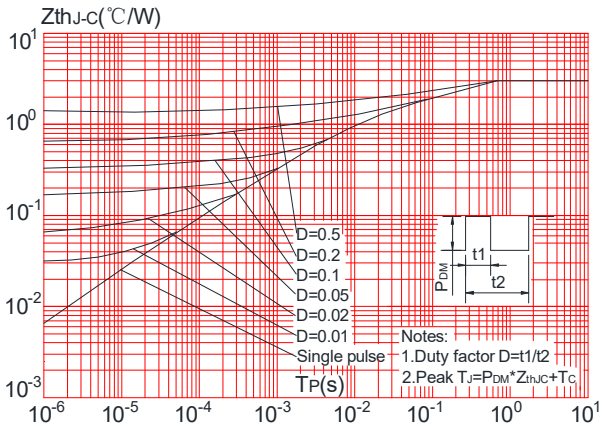


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit and Waveform

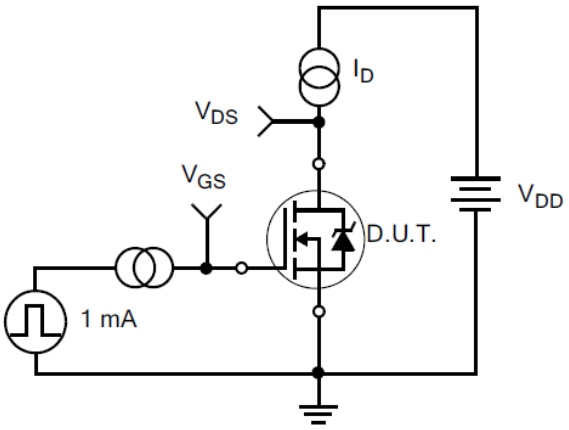


Figure 17. Gate Charge Test Circuit

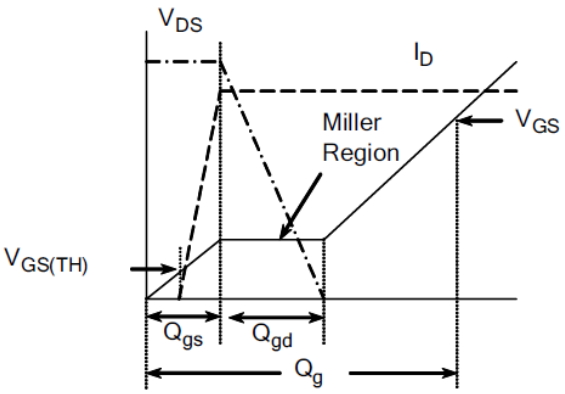


Figure 18. Gate Charge Waveform

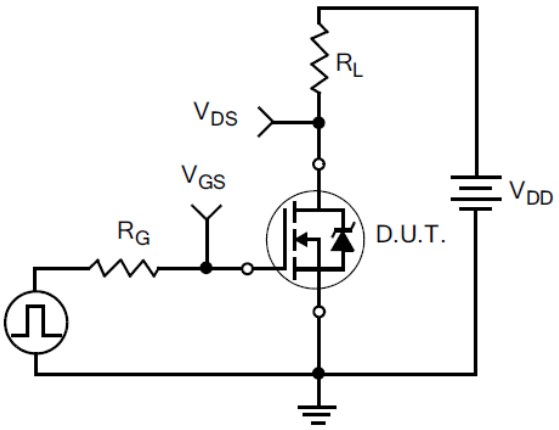


Figure 19. Resistive Switching Test Circuit

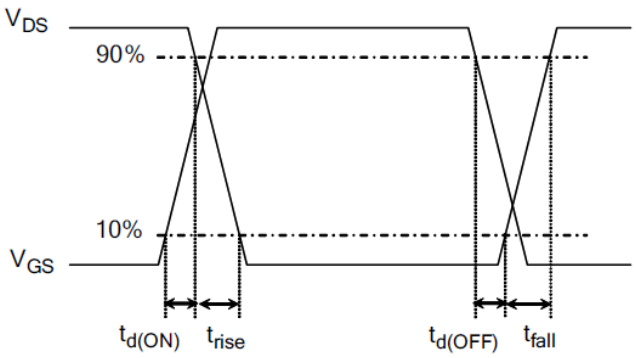


Figure 20. Resistive Switching Waveforms

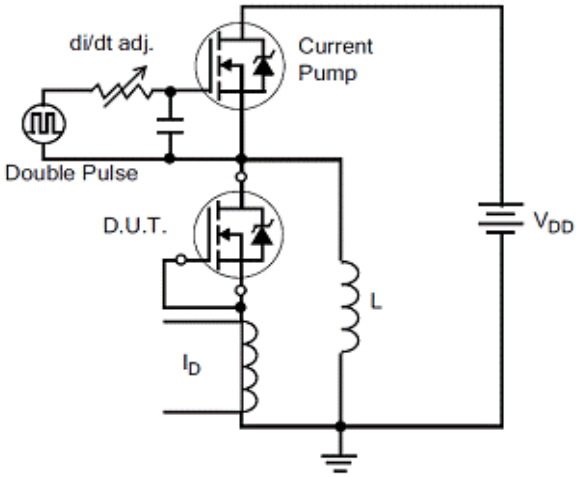


Figure 21. Diode Reverse Recovery Test Circuit

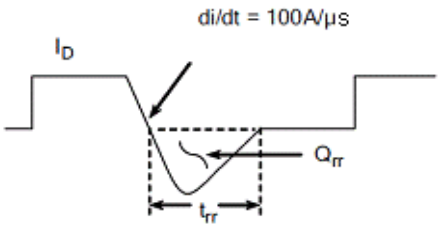


Figure 22. Diode Reverse Recovery Waveform

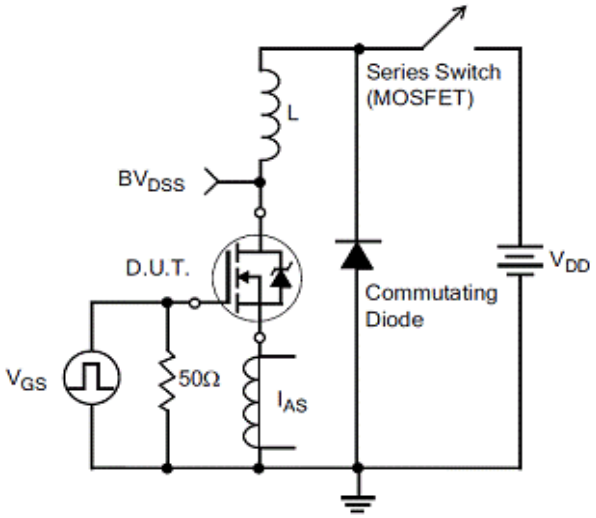


Figure 23. Unclamped Inductive Switching Test Circuit

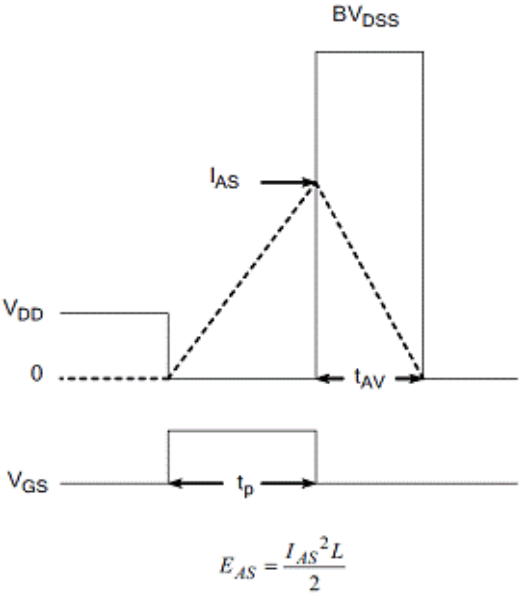
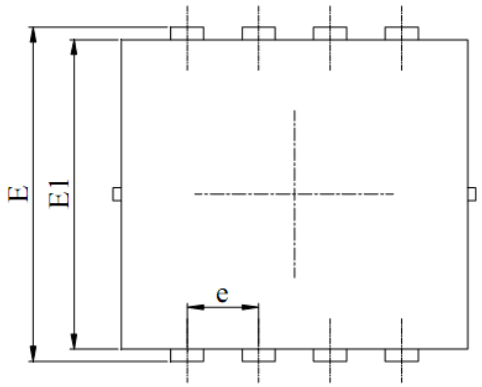
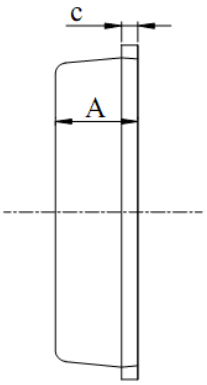


Figure 24. Unclamped Inductive Switching Waveforms

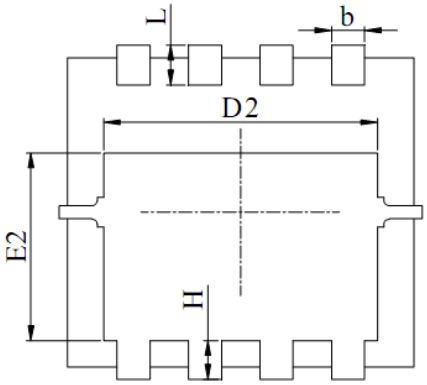
Package Mechanical Data-PDFN3333-8L-Single



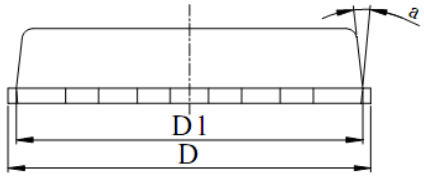
Top View



Side View



Bottom View

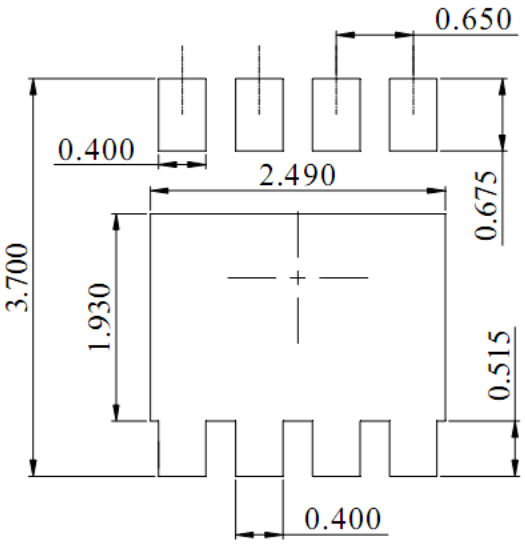


Front View

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS