Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Product Summary

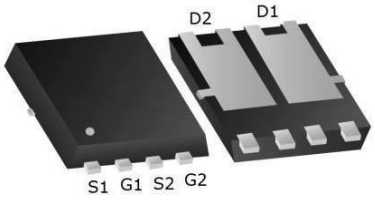
Green

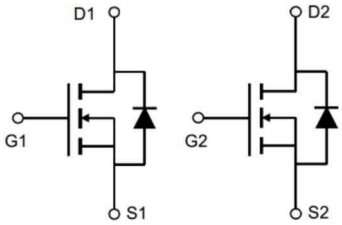
BVDSS	RDSON	ID
60V	11mΩ	25A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

PDFN3333-8L Pin Configuration





Absolute Maximum Ratings（T_A = 25°C, unless otherwise noted）

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	25	A
	T_C=100°C		18	
Pulsed Drain Current[1]		I_{DM}	136	A
Single Pulse Avalanche Energy[2]		EAS	33.8	mJ
Total Power Dissipation	T_C=25°C	P_D	27	W
Operating Junction and Storage Temperature Range		T_J , T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[3]	$R_{\theta JA}$	55	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	4.6	°C/W

Electrical Characteristics（T_J = 25°C, unless otherwise noted）

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60	-	-	V
Gate-Body Leakage Current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} = 65V, V_{GS} = 0V	-	-	1	μA
	T_J=100°C			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.7	2.2	V
Drain-Source on-Resistance[4]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	11	14	mΩ
			V_{GS} = 4.5V, I_D = 10A	-	14	19	
Forward Transconductance[4]		g_{fs}	V_{DS} = 10V, I_D = 20A	-	42	-	S
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = 30V, V_{GS} =0V, f =1MHz	-	738	-	pF
Output Capacitance		C_{oss}		-	225	-	
Reverse Transfer Capacitance		C_{rss}		-	13.5	-	
Gate Resistance		R_G	f =1MHz	-	1.2	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = 10V, V_{DS} = 30V, I_D= 20A	-	14	-	nC
Gate-Source Charge		Q_{gs}		-	2.6	-	
Gate-Drain Charge		Q_{gd}		-	2.9	-	
Turn-on Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DD}= 30V, R_G = 3Ω, I_D= 20A	-	5.7	-	ns
Rise Time		t_r		-	5.1	-	
Turn-off Delay Time		$t_{d(off)}$		-	14.8	-	
Fall Time		t_f		-	4.6	-	
Body Diode Reverse Recovery Time		t_{rr}	I_F = 20A, dI/dt = 100A/μs	-	24	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	9.6	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = 20A, V_{GS} = 0V	-	-	1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	25	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The test condition is V_{DD}= 25V, V_{GS}= 10V, L= 0.4mH, I_{AS}= 13A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

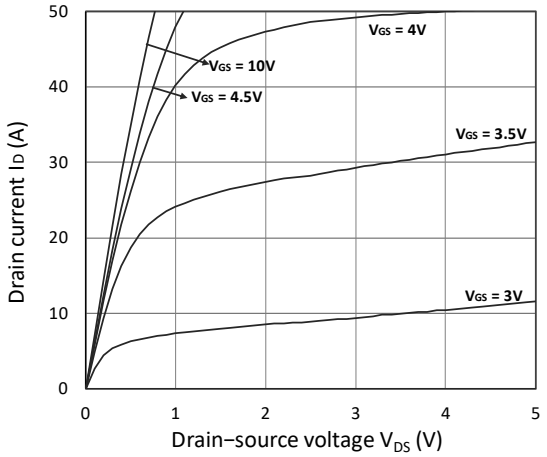


Figure 1. Output Characteristics

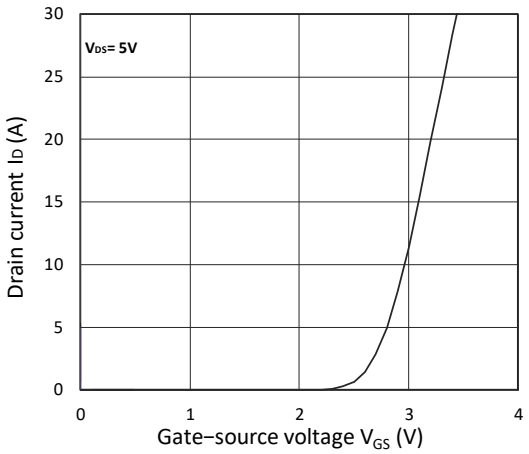


Figure 2. Transfer Characteristics

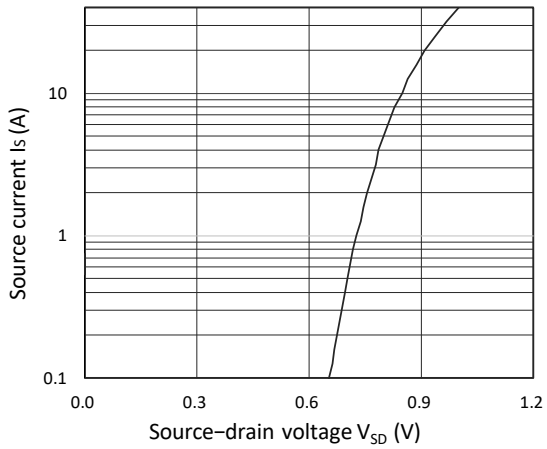


Figure 3. Forward Characteristics of Reverse

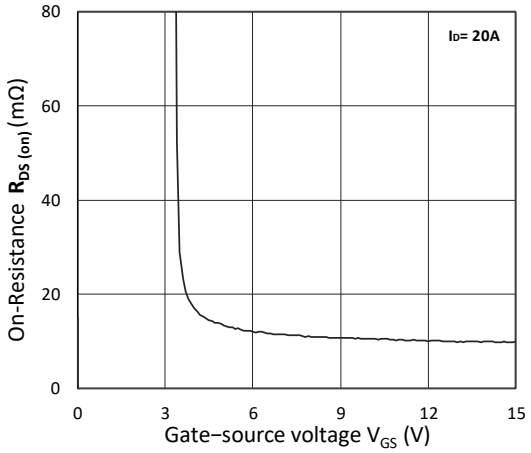


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

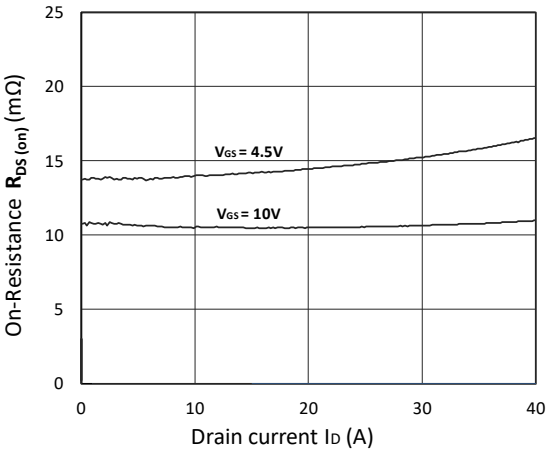


Figure 5. $R_{DS(ON)}$ vs. I_D

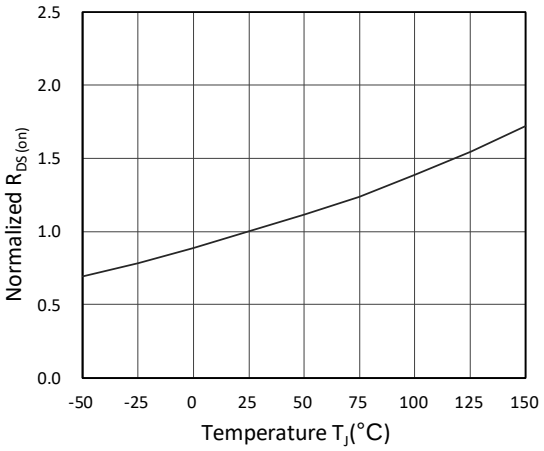


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

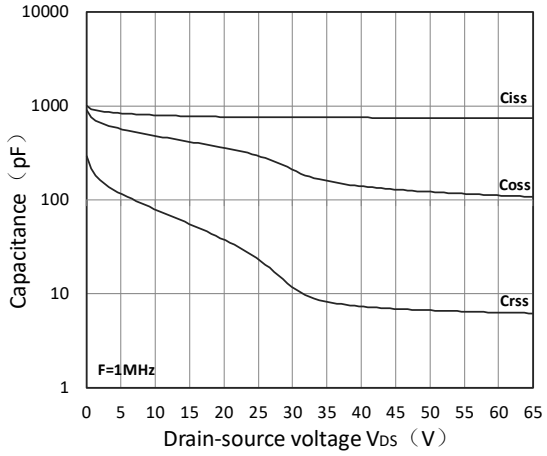


Figure 7. Capacitance Characteristics

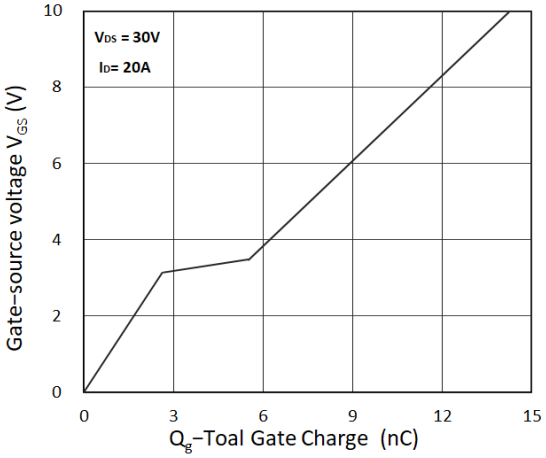


Figure 8. Gate Charge Characteristics

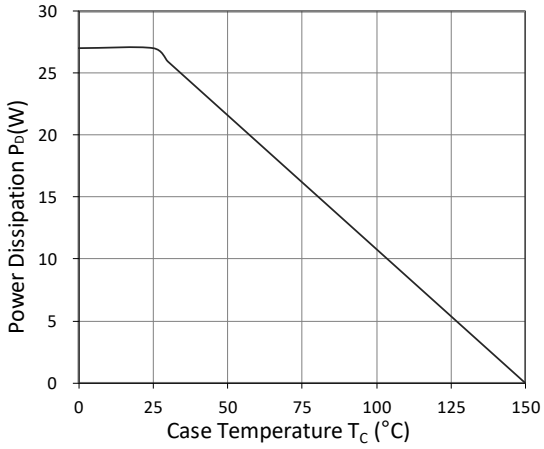


Figure 9. Power Dissipation

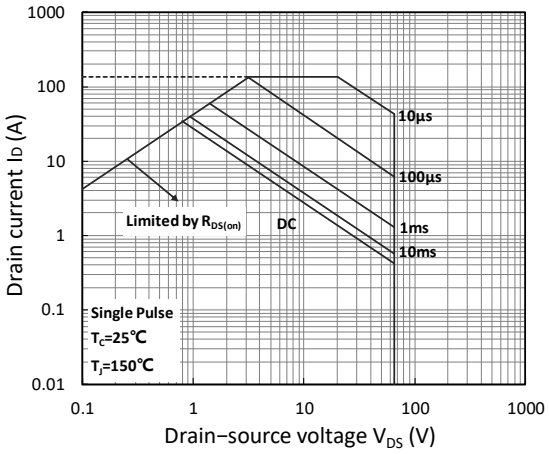


Figure10. Safe Operating Area

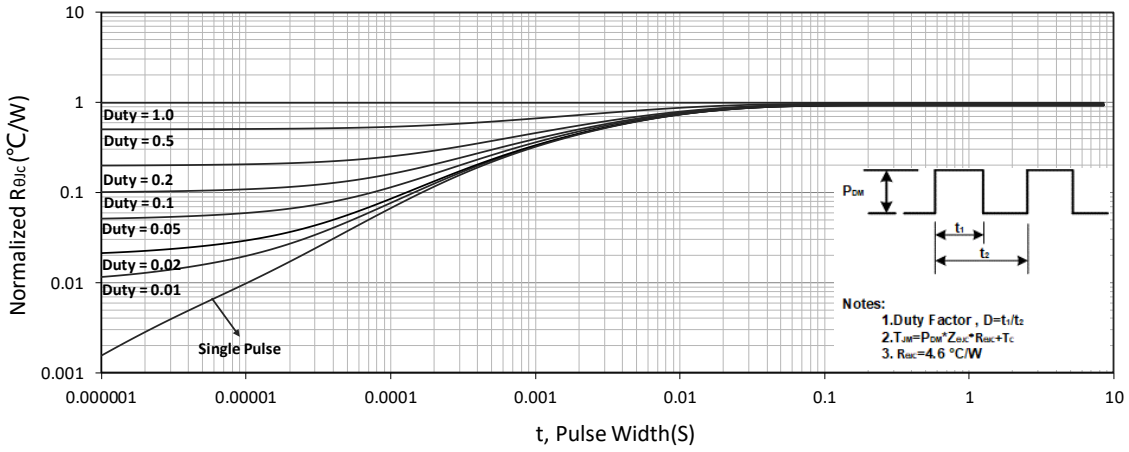
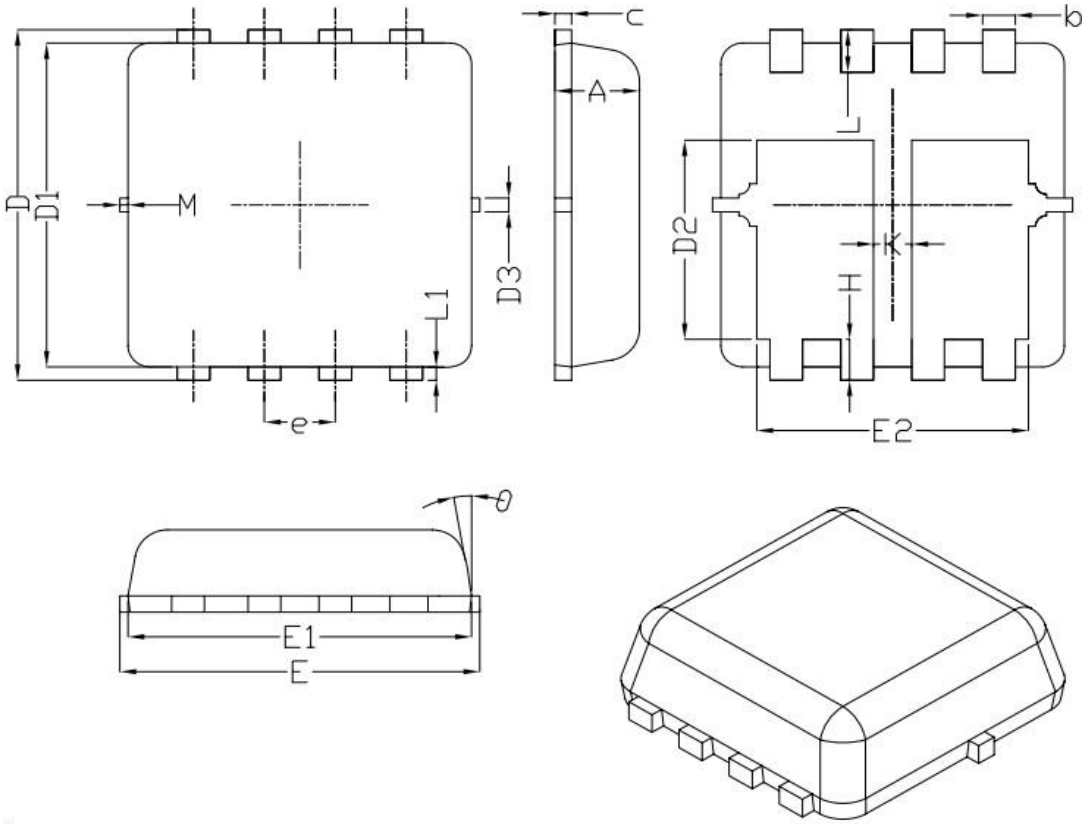


Figure 11. Normalized Maximum Transient Thermal Impedance

Dual PDFN3333-8L Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:
1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.