

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

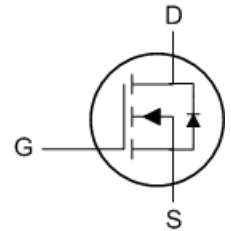
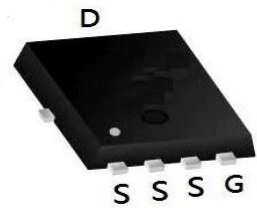
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

Product Summary



BVDSS	RDSON	ID
40V	1.1mΩ	225A

PDFN5060-8L Pin Configuration

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current (Silicon limited)		I_D	225	A
Drain Current ^A	$T_C=25^\circ\text{C}$	I_D	130	A
	$T_C=100^\circ\text{C}$		82	
Pulsed Drain Current ^B		I_{DM}	390	A
Avalanche energy ^C		E_{AS}	450	mJ
Total Power Dissipation ^D		P_D	114	W
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.1	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient ^E		$R_{\theta JA}$	20	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

N-Ch 40V Fast Switching MOSFETs

■ Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	40	48		V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V,V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.2	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A		1.1	1.4	mΩ
		V _{GS} = 4.5V, I _D =20A		1.7	2.3	
Gate Resistance	R _g	V _{GS} =0V,V _{DS} Open,f=1MHZ		2.7		Ω
Maximum Body-Diode Continuous Current	I _S				100	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V,f=300KHZ		8300		pF
Output Capacitance	C _{oss}			1510		
Reverse Transfer Capacitance	C _{rss}			130		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V,V _{DS} =32V,I _D =20A		127		nC
Gate-Source Charge	Q _{gs}			35		
Gate-Drain Charge	Q _{gd}			26		
Reverse Recovery Chrage	Q _{rr}	I _F =25A, di/dt=100A/us		163		ns
Reverse Recovery Time	t _{rr}			100		
Turn-on Delay Time	t _{d(on)}	V _{GS} =10V,V _{DD} =20V,I _D =25A R _{GEN} =2Ω		22.5		
Turn-on Rise Time	t _r			6.7		
Turn-off Delay Time	t _{d(off)}			80.3		
Turn-off fall Time	t _f			26.9		

Note:

- The maximum current rating is package limited.
- Repetitive rating; pulse width limited by max. junction temperature.
- $V_{DD}=32V, R_G=25\Omega, L=0.5\text{mH}$, starting $T_J=25^{\circ}\text{C}$.
- P_D is based on max. junction temperature, using junction-case thermal resistance.
- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25^{\circ}\text{C}$.

■ Typical Performance Characteristics

Figure.1 Typical Output Characteristics

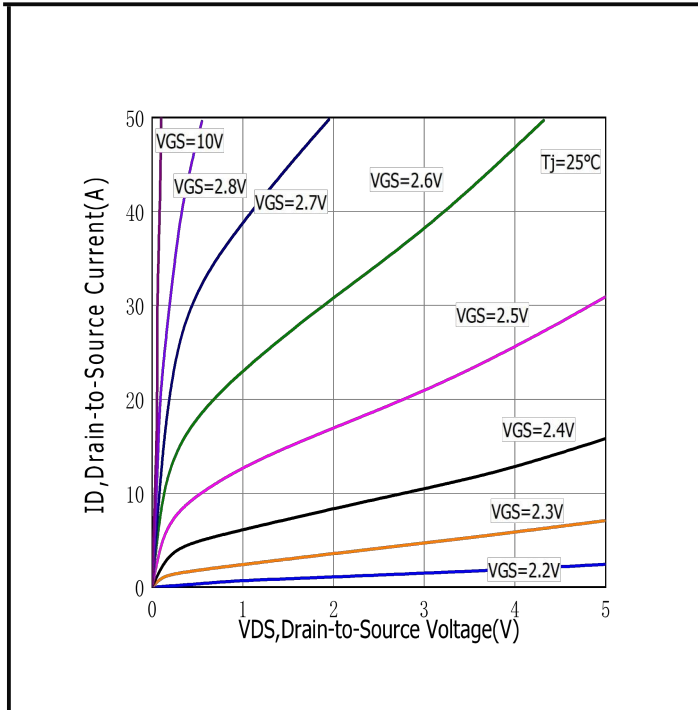


Figure.2 Typical Gate Charge vs Gate to Source Voltage

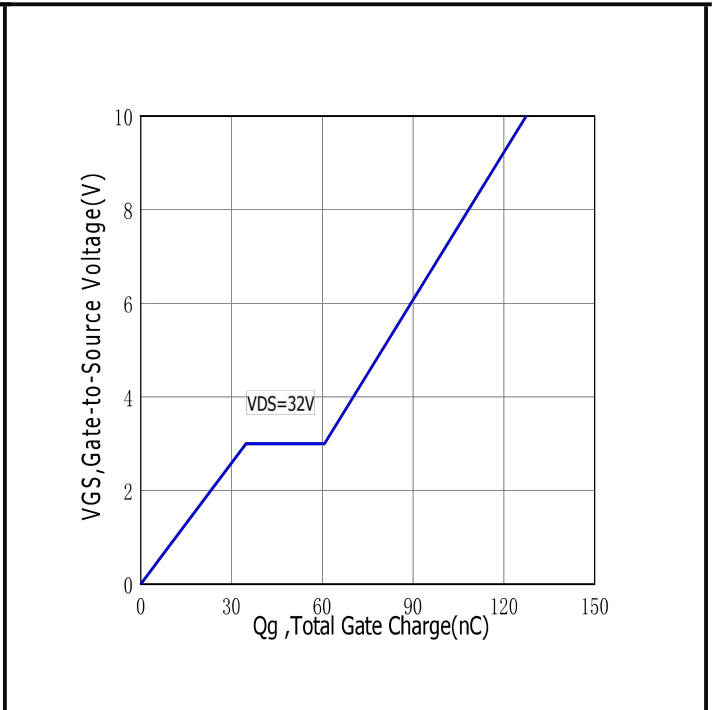


Figure.3 Typical Body Diode Transfer Characteristics

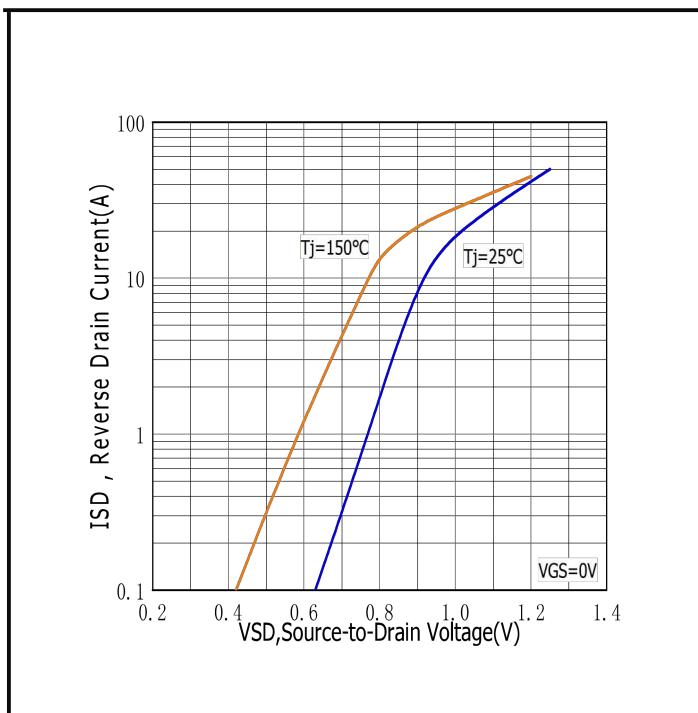


Figure.4 Typical Capacitance vs Drain to Source Voltage

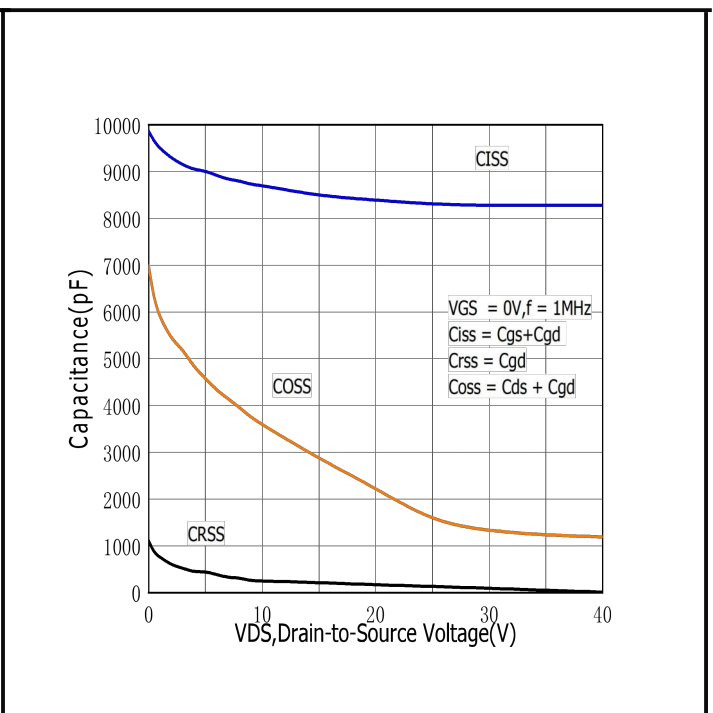


Figure.5 Typical Breakdown Voltage vs Junction Temperature

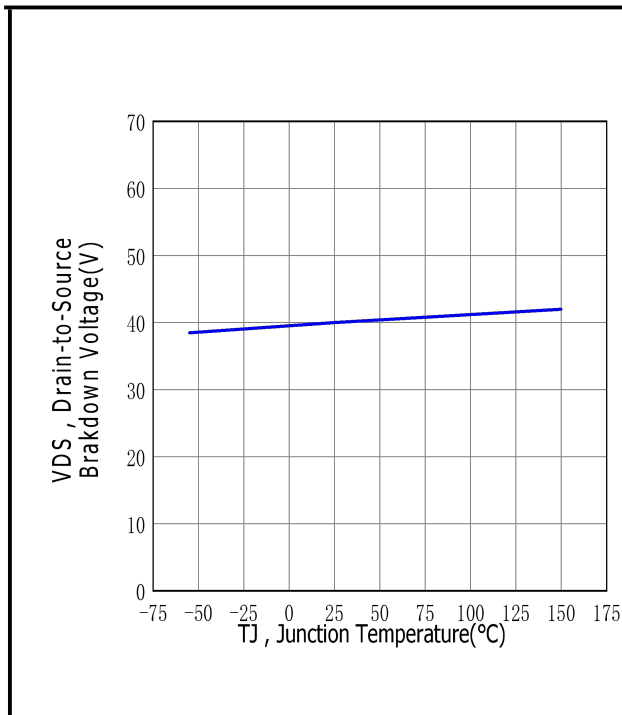


Figure.6 Typical Drain to Source on Resistance vs Junction Temperature

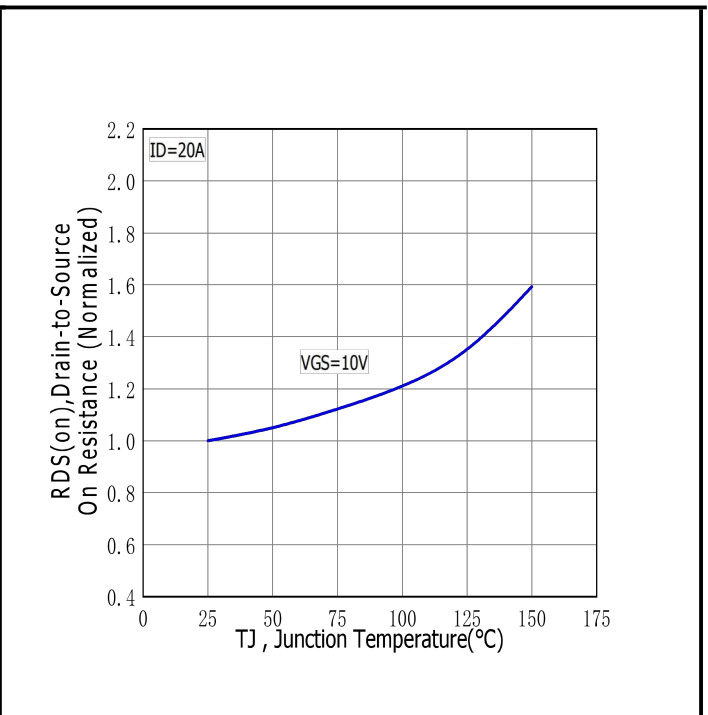


Figure.7 Maximum Forward Bias Safe Operating Area

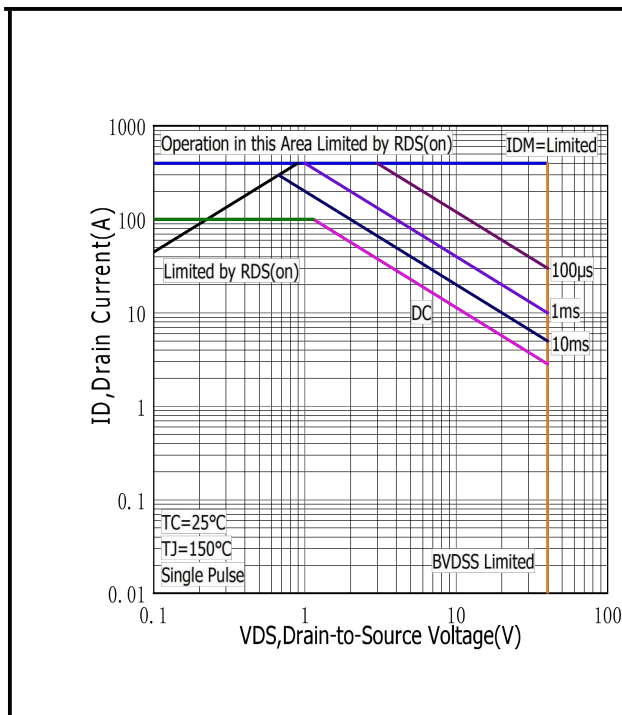
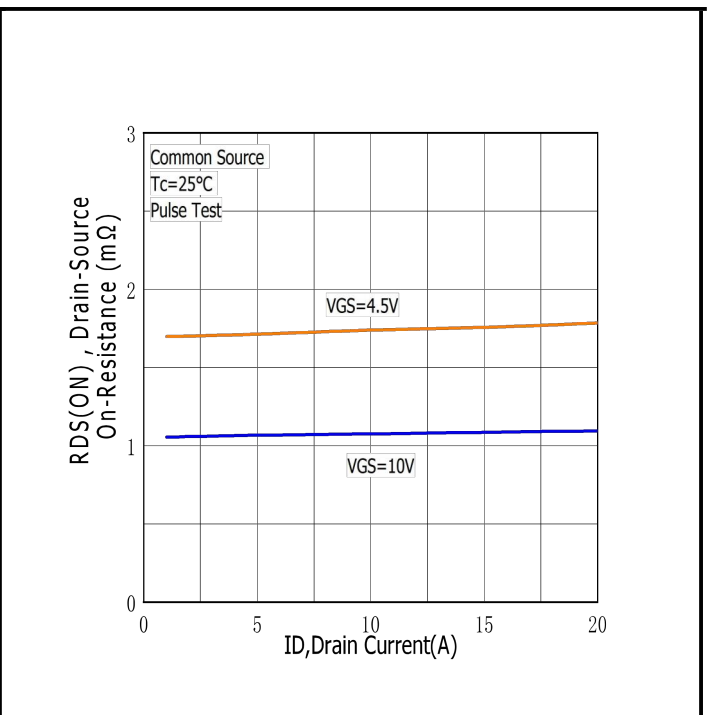


Figure.8 Typical Drain to Source ON Resistance vs Drain Current



■ Typical Performance Characteristics

Figure.9 Maximum EAS vs Channel Temperature

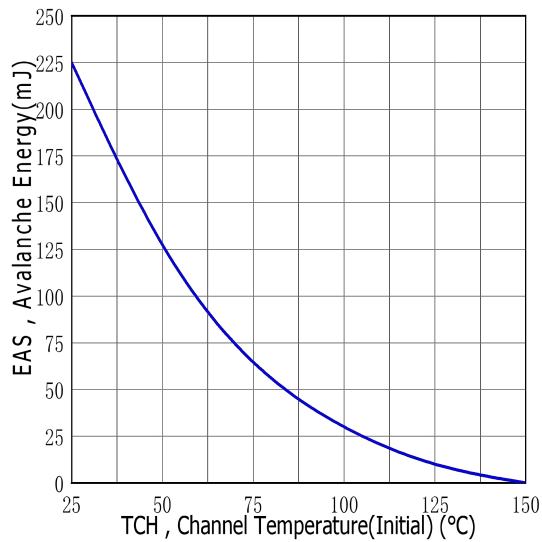


Figure.10 Typical Threshold Voltage vs Case Temperature

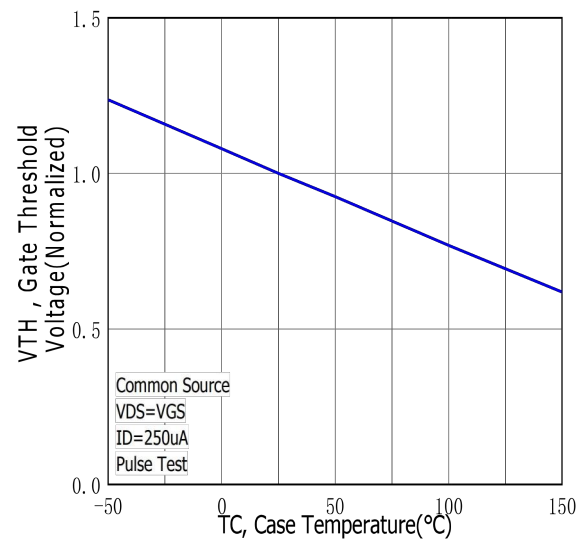


Figure.11 Typical Transfer Characteristics

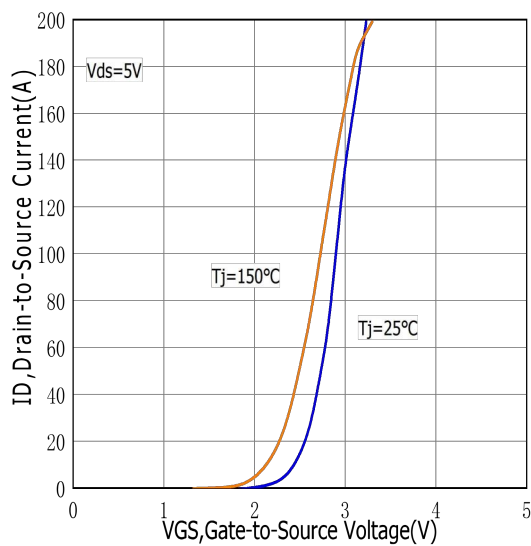


Figure.12 Maximum Power Dissipation vs Case Temperature

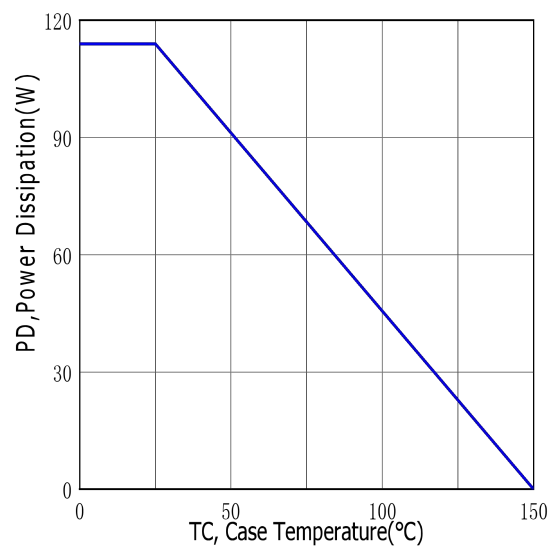
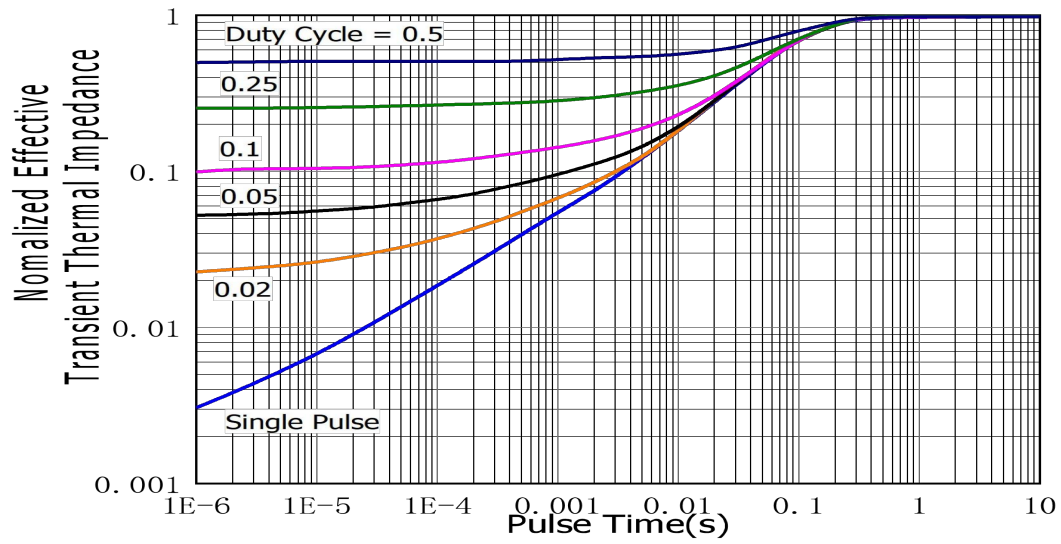


Figure.13 Maximum Effective Thermal Impedance , Junction to Case



■ Test circuits and waveforms

N-Ch 40V Fast Switching MOSFETs

Figure A: Gate Charge Test Circuit & Waveforms

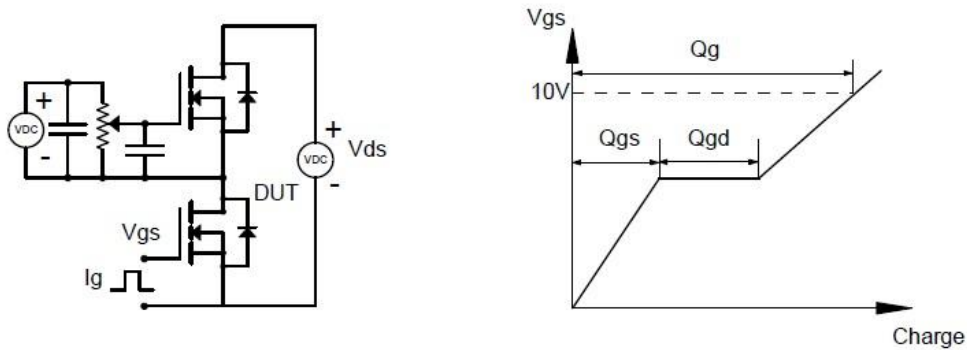


Figure B: Resistive Switching Test Circuit & Waveforms

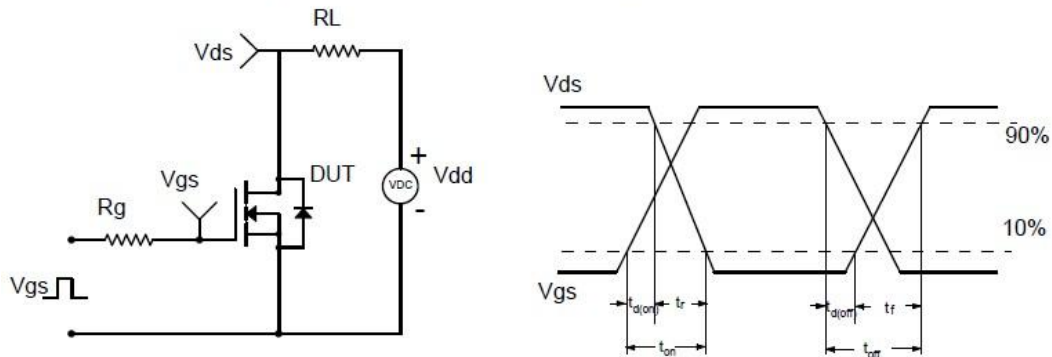


Figure C: Unclamped Inductive Switching (UIS) Test

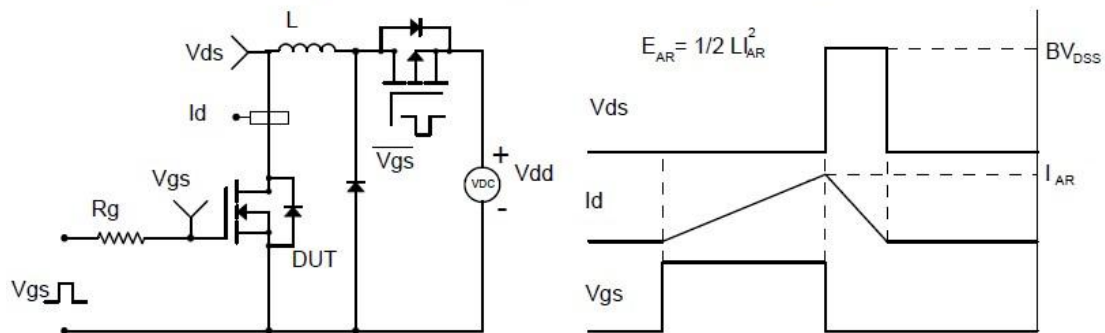
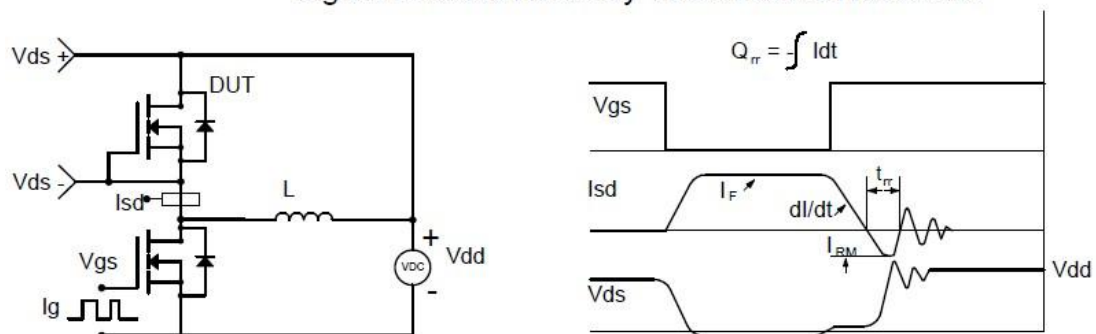
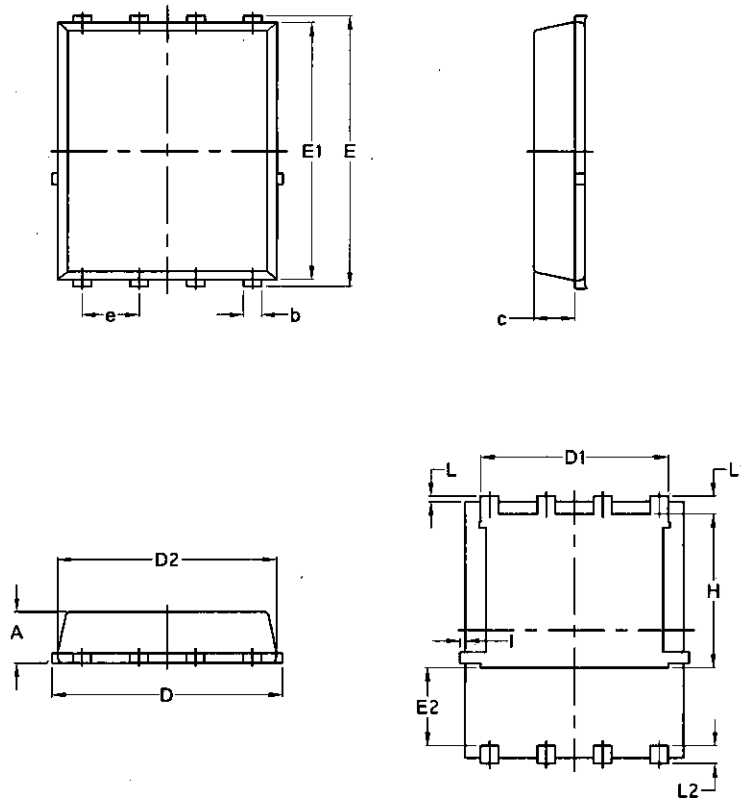


Figure D: Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-PDFN5060-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070