P-Ch 60V Fast Switching MOSFETs

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Product Summary

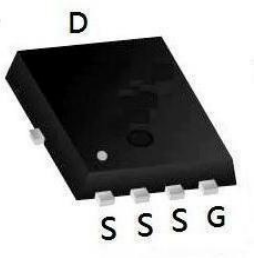
Green

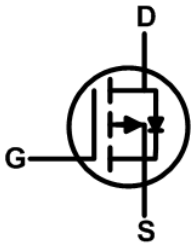
BVDSS	RDSON	ID
-60V	5.5 mΩ	-100A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

PDFN5060-8L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	-100	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	-70	A
I_{DM}	Pulsed Drain Current[2]	-440	A
EAS	Single Pulse Avalanche Energy[3]	960	mJ
I_{AS}	Avalanche Current	---	A
P_D@T_C=25℃	Total Power Dissipation[4]	180	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	60	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	0.69	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-60	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	---	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-15A	---	5.5	7.2	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.6	-2.0	-2.4	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-60V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-60, V_{GS}=0V , T_J=100℃	---	---	-100	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-10V , I_D=-30A	---	---	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2	---	Ω
Q_g	Total Gate Charge	V_{DS}=-30 , V_{GS}=-10V , I_D=-15A	---	80.2	---	nC
Q_{gs}	Gate-Source Charge		---	15.2	---	
Q_{gd}	Gate-Drain Charge		---	11	---	
$T_{d(on)}$	Turn-On Delay Time	VGS=-10V, VDD=-30V, RG=3Ω, ID=-15A	---	4.5	---	ns
T_r	Rise Time		---	2.5	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14.5	---	
T_f	Fall Time		---	3.5	---	
C_{iss}	Input Capacitance	V_{DS}=-30V , V_{GS}=0V , f=1MHz	---	5403	---	pF
C_{oss}	Output Capacitance		---	941	---	
C_{rss}	Reverse Transfer Capacitance		---	48	---	

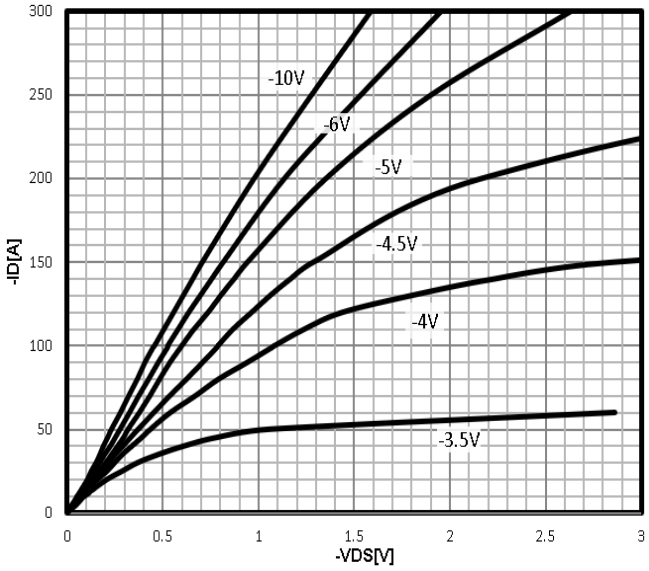
Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-100	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-15A , T_J=25℃	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	IF=-15A , di/dt=100A/μs , T_J=25℃	---	60	---	nS
Q_{rr}	Reverse Recovery Charge		---	105	---	nC

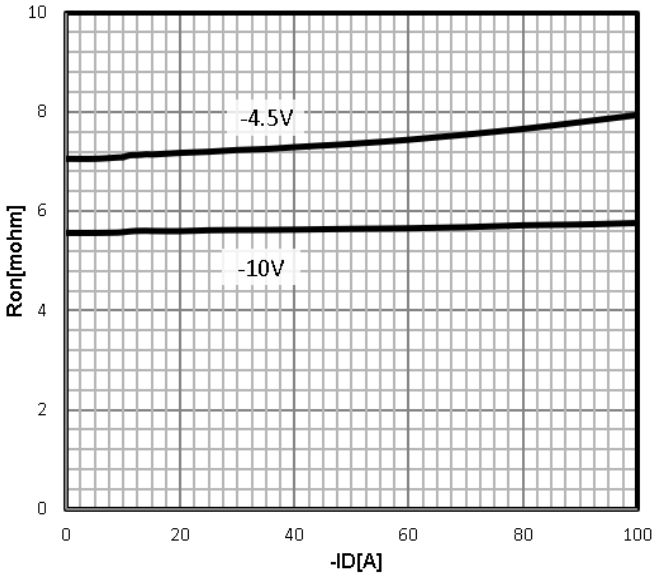
Note :
1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is TJ = C,VDD=-30V,VGS=-10V,L=0.5mH
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Characteristics Curve:

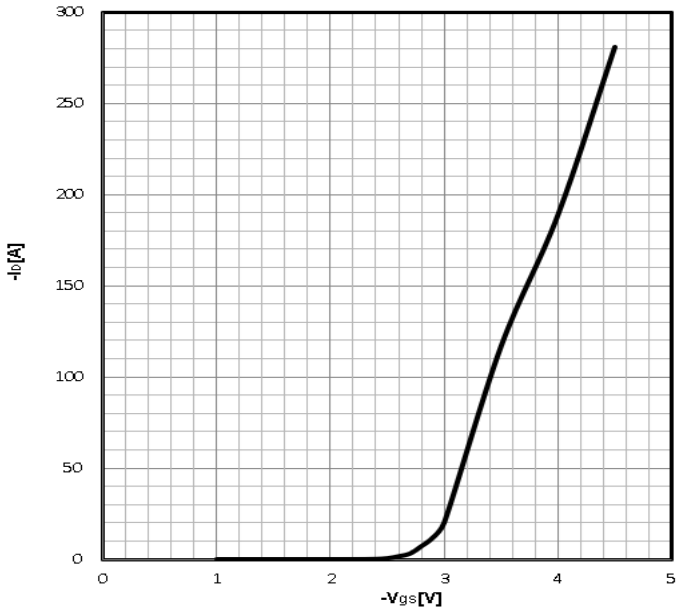
Typ. output characteristics
$I_D=f(V_{DS})$



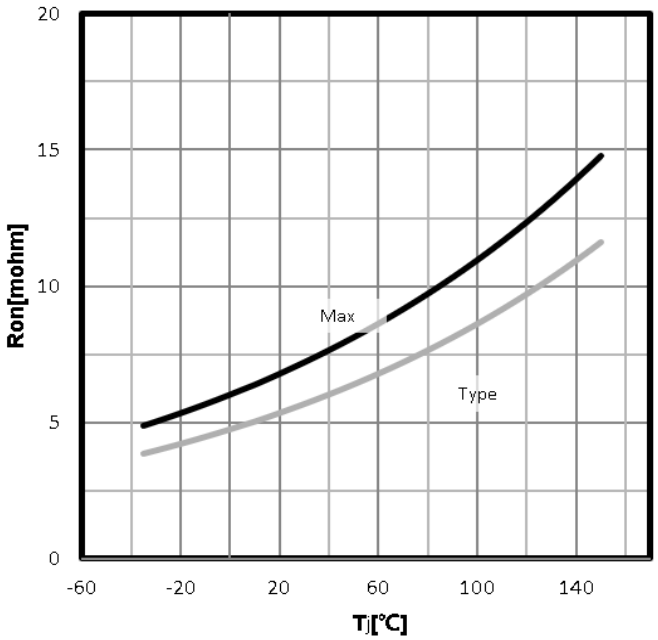
Typ. drain-source on resistance
$R_{DS(on)}=f(I_D)$



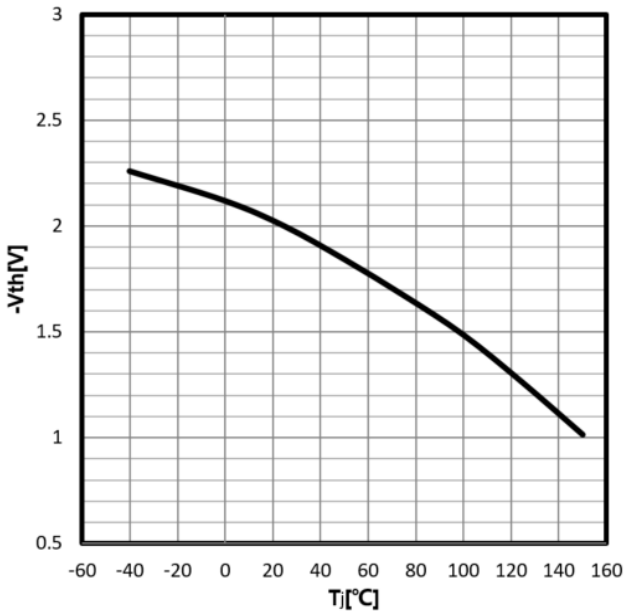
Typ. transfer characteristics
$I_D=f(V_{GS})$



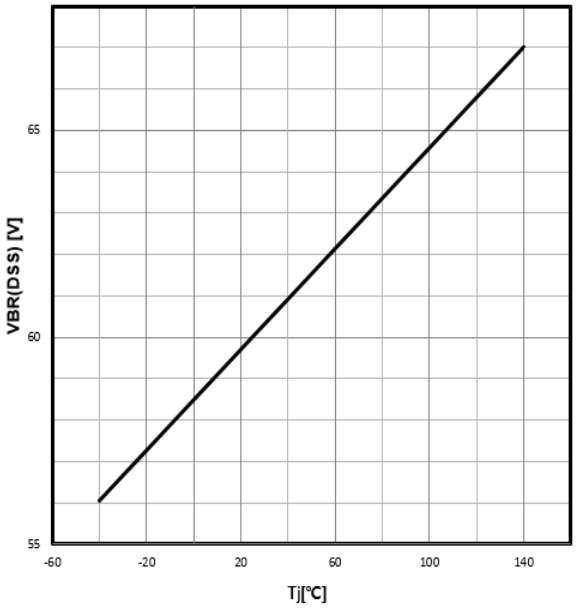
Drain-source on-state resistance
$R_{DS(on)}=f(T_j);I_D=-15A;\ V_{GS}=-10V$



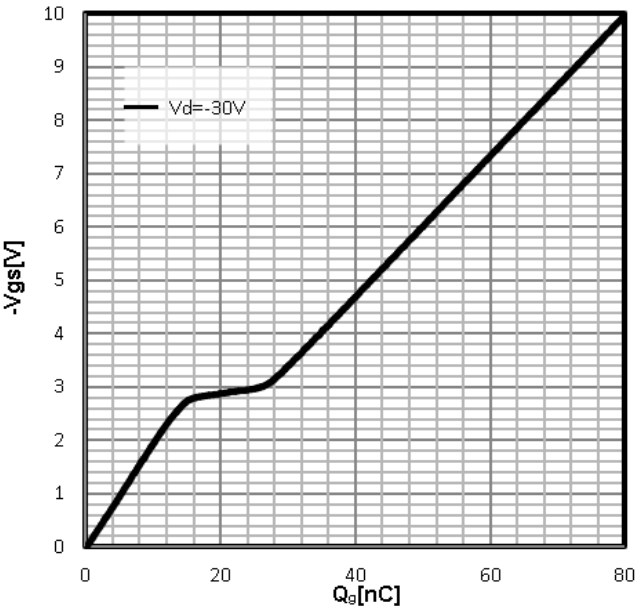
Gate Threshold Voltage -
$V_{TH}=f(T_j)$; I_D=-250uA



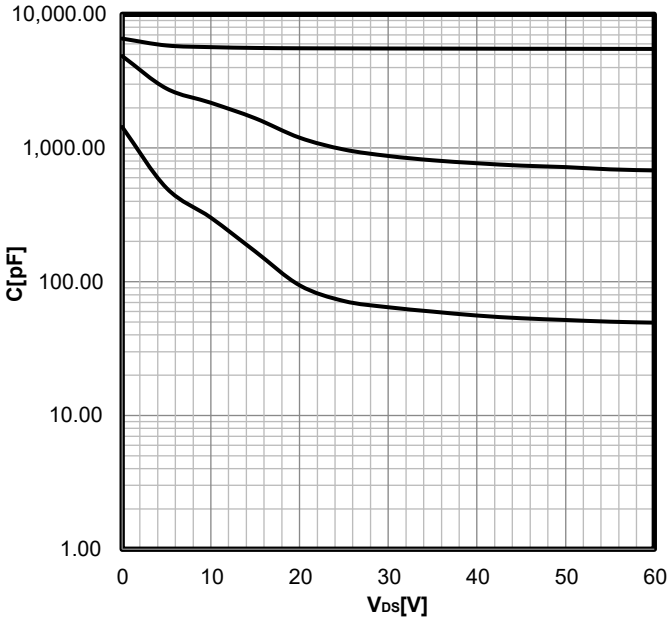
Drain-source breakdown voltage
$V_{BR(DSS)}=f(T_j)$; I_D=-250uA



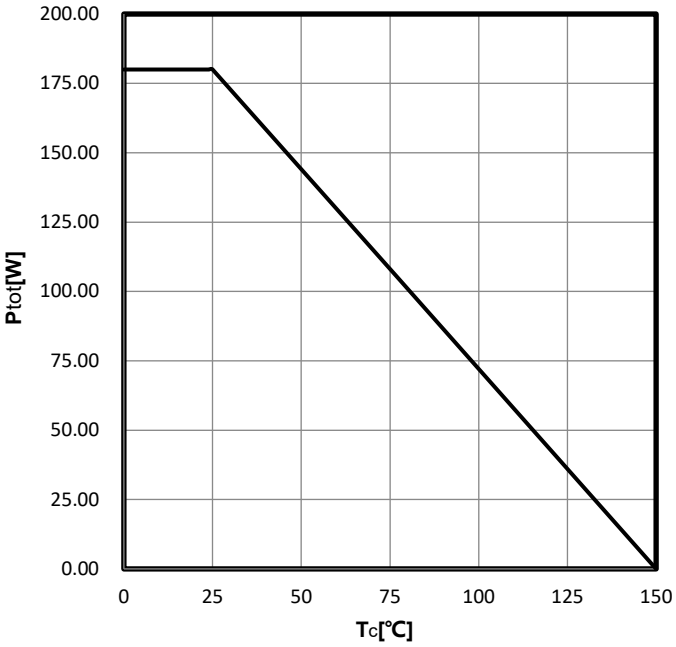
Typ. gate charge
$V_{GS}=f(Q_{gate})$; I_D=-15A



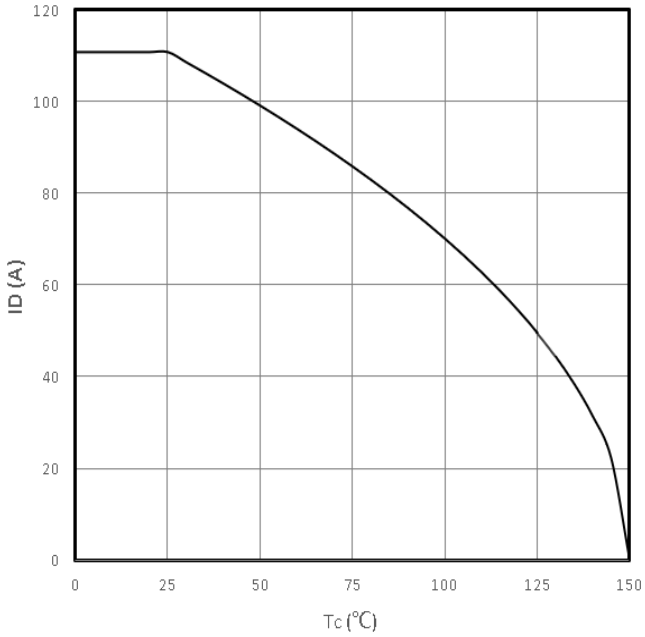
Typ. capacitances
C =f(V_{DS}); V_{GS}=0V; f =1MHz



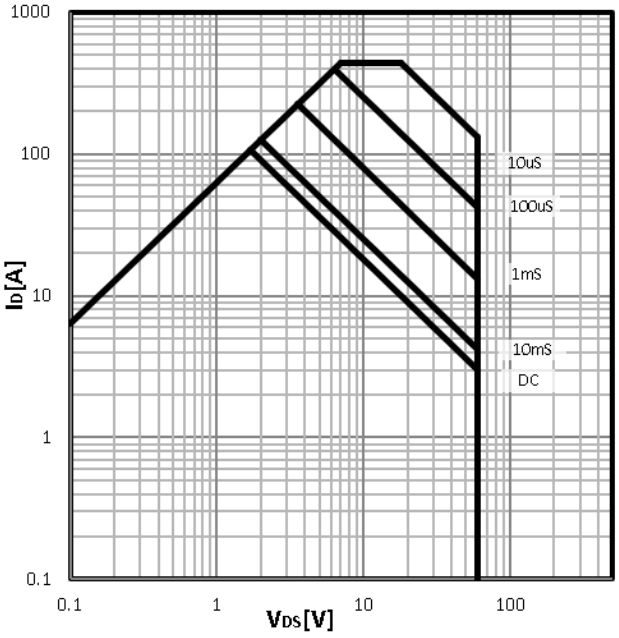
Power Dissipation
$P_{tot}=f(T_C)$



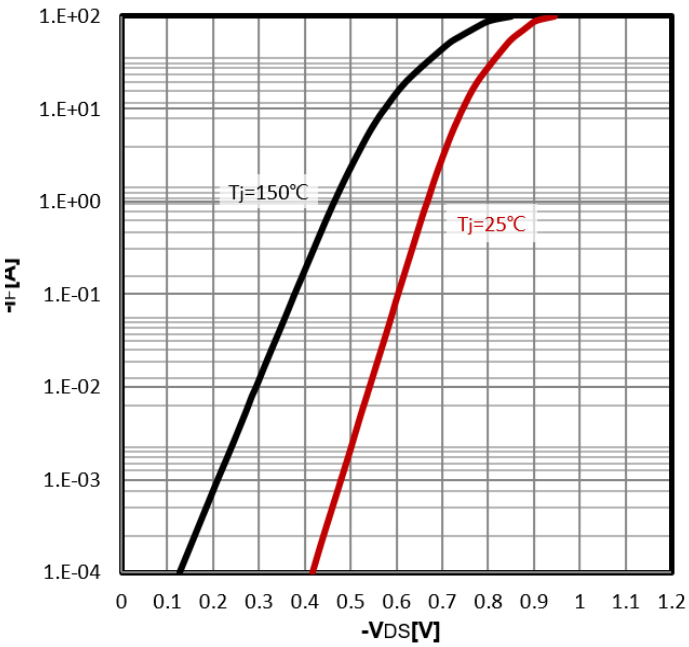
Maximum Drain Current
$-I_D=f(T_C)$



Safe operating area
$I_D=f(V_{DS})$

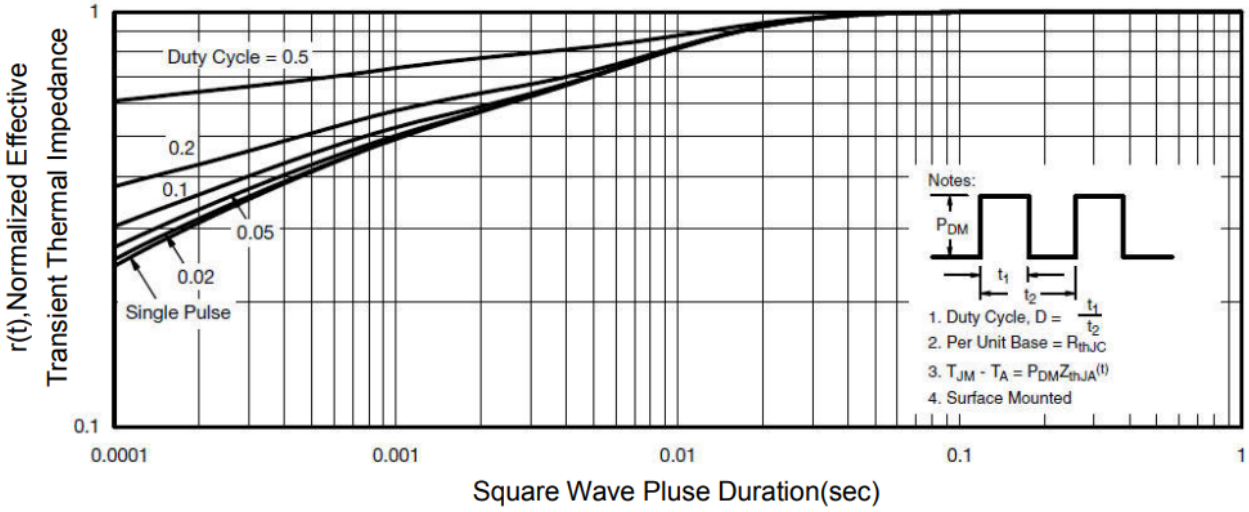


Body Diode Forward Voltage Variation
$-I_F=f(-V_{DS})$



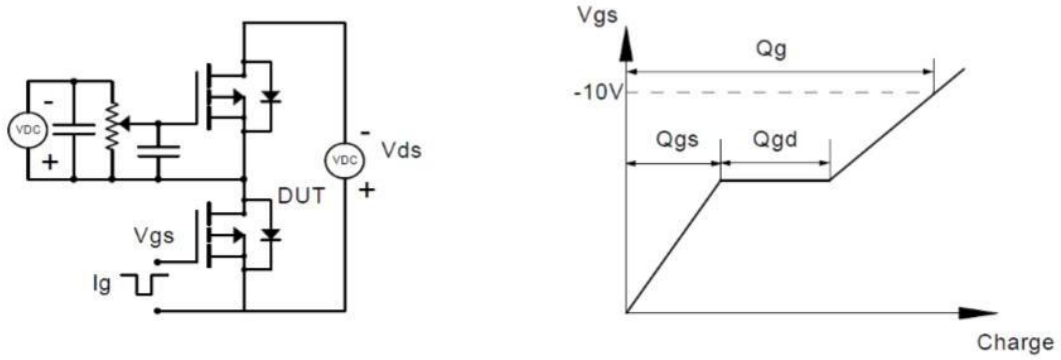
Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

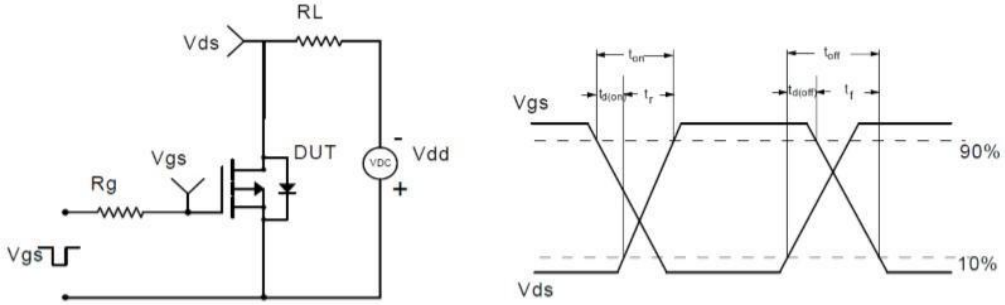


Test Circuit and Waveform:

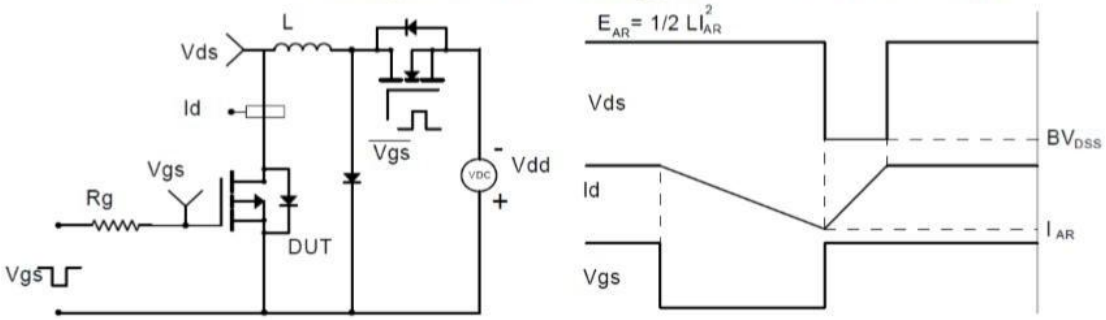
Gate Charge Test Circuit & Waveform



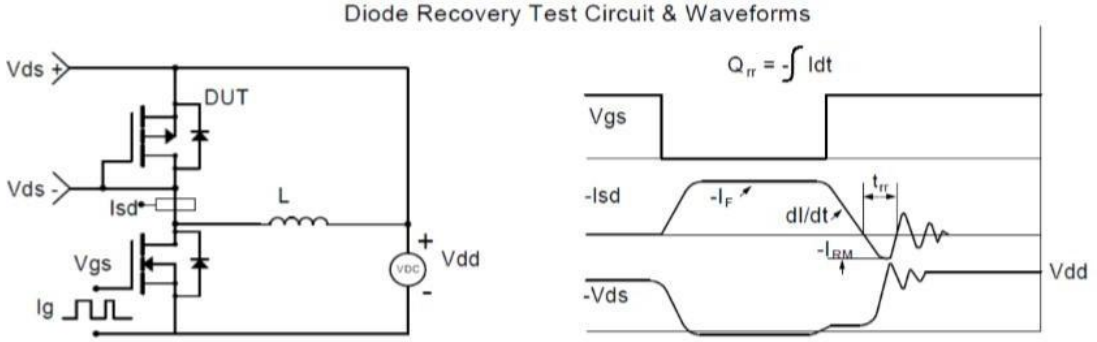
Resistive Switching Test Circuit & Waveforms



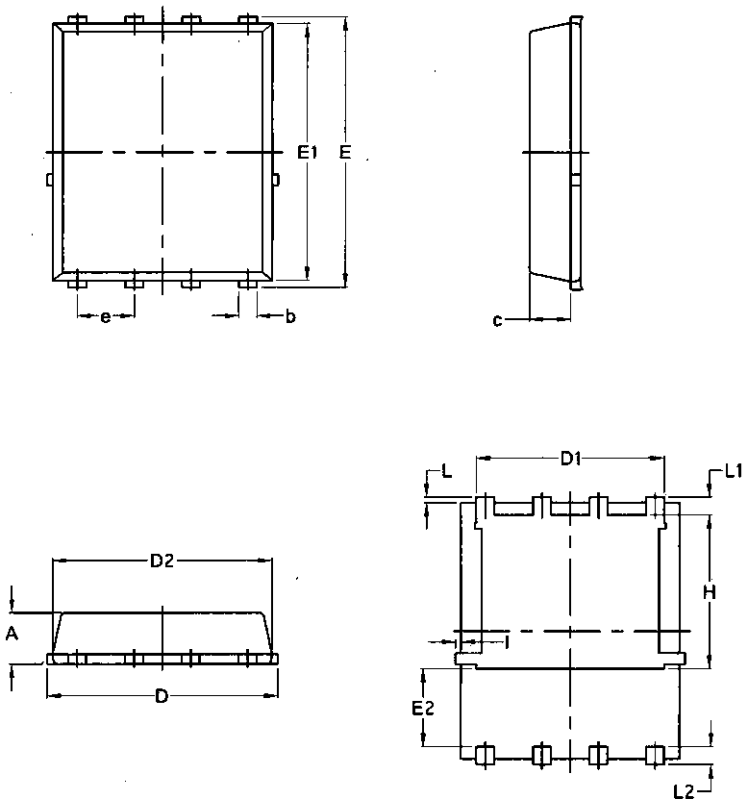
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-PDFN5060-8L-Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070