

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

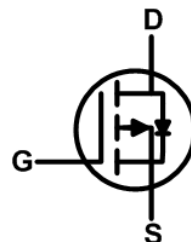
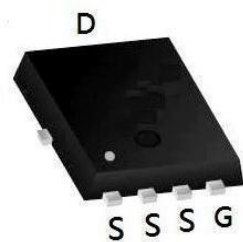
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

Product Summary



BVDSS	RDSON	ID
-100V	72mΩ	-18A

PDFN3333-8L Pin Configuration



Absolute Maximum Ratings:

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		-100	V
I_D	Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	-18	A
	Continuous Drain Current	$T_C = 100\text{ }^{\circ}\text{C}$	-13	A
I_{DM}^{a1}	Pulsed Drain Current		-80	A
E_{AS}^{a2}	Single pulse avalanche energy		200	mJ
V_{GS}	Gate-to-Source Voltage		± 20	V
P_D	Power Dissipation		80	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range		150, -55 to 150	$^{\circ}\text{C}$
T_L	Maximum Temperature for Soldering		260	$^{\circ}\text{C}$

Thermal Characteristics:

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.56	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	91	$^{\circ}\text{C/W}$

Electrical Characteristics (TA= 25°C unless otherwise specified) :

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-100	--	--	V
I _{DSS}	Drain to Source Leakage Current	V _{DS} =-100V, V _{GS} =0V	--	--	1	μA
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} =-20V, V _{DS} =0V	--	--	100	nA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} =+20V, V _{DS} =0V	--	--	-100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.5	-2.0	-2.5	V
R _{DS(ON)1}	Drain-to-Source Resistance	On- V _{GS} =-10V, I _D =-10A	--	72	89	mΩ
R _{DS(ON)2}	Drain-to-Source Resistance	On- V _{GS} =-4.5V, I _D =-5A	--	87	105	mΩ

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = -50V f = 1.0MHz	--	1305	--	pF
C _{oss}	Output Capacitance		--	97.5	--	
C _{rss}	Reverse Transfer Capacitance		--	9.1	--	
R _g	Gate resistance	V _{GS} = 0V, V _{DS} Open	--	75	--	Ω

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	I _D = -10A V _{DS} = -50V V _{GS} = -10V R _G = 5Ω	--	8.8	--	ns
t _r	Rise Time		--	16	--	
t _{d(OFF)}	Turn-Off Delay Time		--	60	--	
t _f	Fall Time		--	41	--	
Q _g	Total Gate Charge	V _{GS} = -10V	--	22.16	--	nC
Q _{gs}	Gate Source Charge	V _{DS} = -50V	--	4.59	--	
Q _{gd}	Gate Drain Charge	I _D = -10A	--	4.53	--	

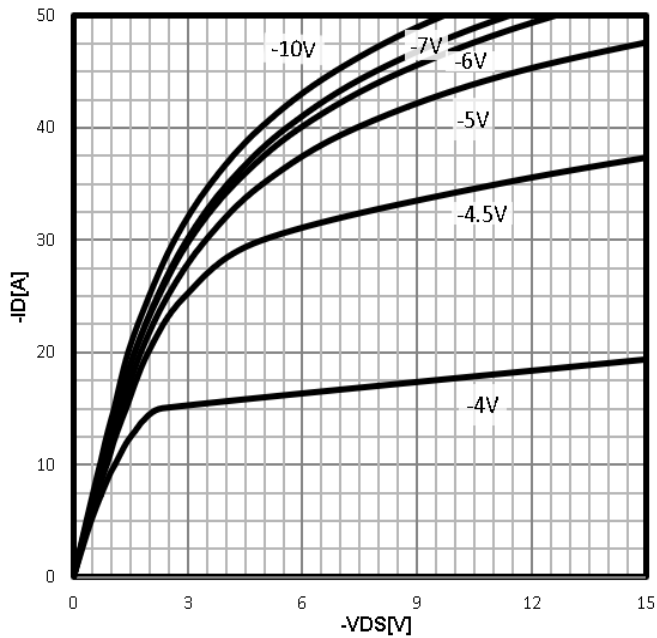
Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V _{SD}	Diode Forward Voltage	I _S =-10A, V _{GS} =0V	--	--	-1.2	V
t _{rr}	Reverse Recovery time	I _S =-10A, V _{DD} =-50V	--	30	--	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	--	61	--	nC

a1 : Repetitive rating; pulse width limited by maximum junction temperature

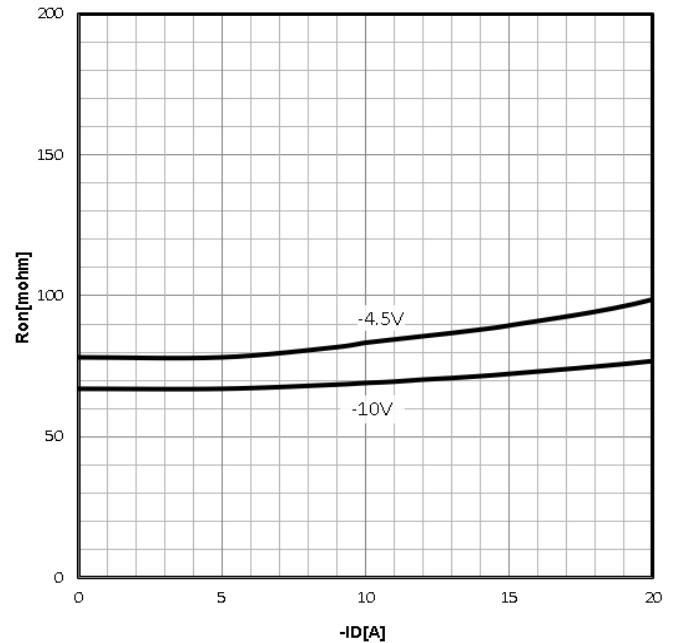
a2 : L=5mH, R_g=25Ω, Starting T_J=25 °C

Characteristics Curve:

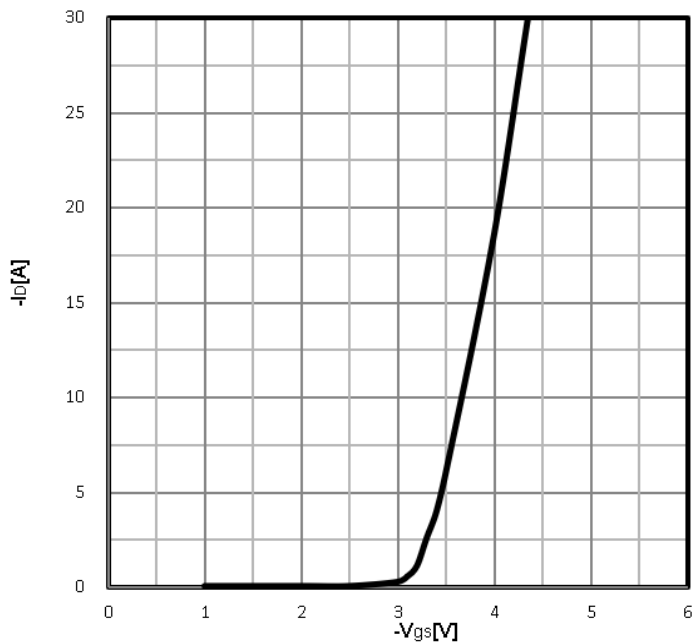
Typ. output characteristics
 $-I_D = f(-V_{DS})$



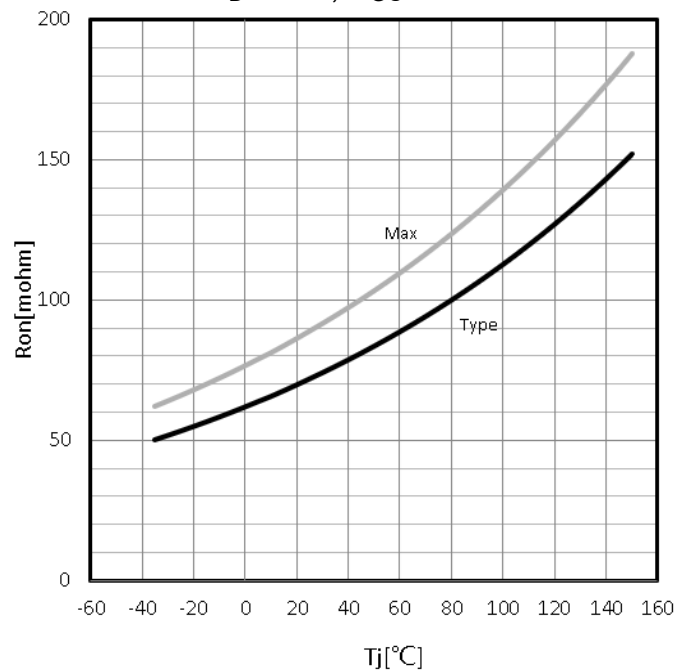
Typ. drain-source on resistance
 $R_{DS(on)} = f(-I_D)$



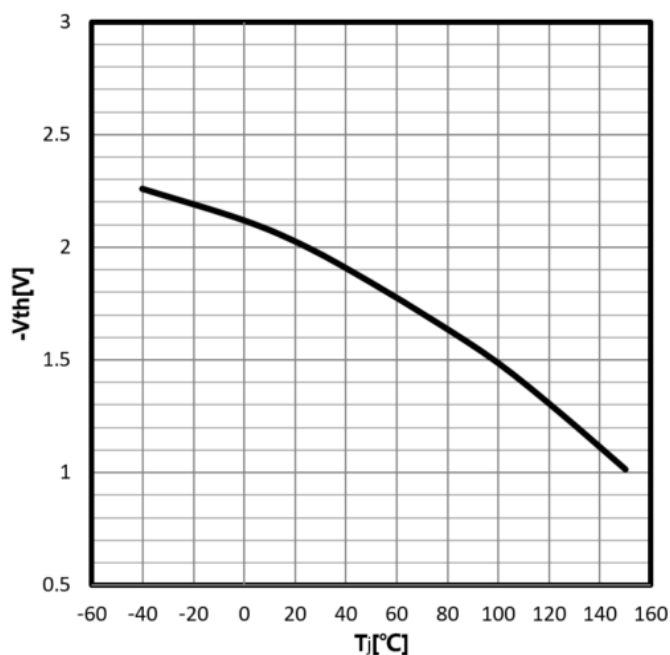
Typ. transfer characteristics
 $-I_n = f(-V_{GS})$



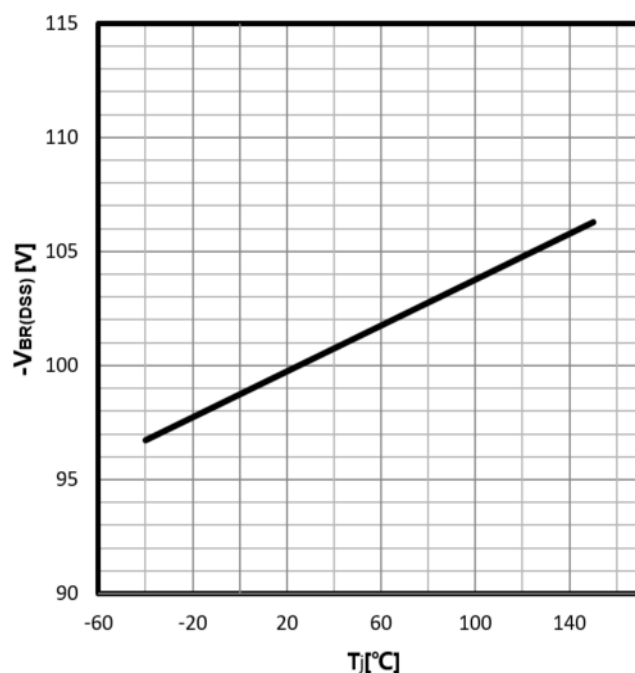
Drain-source on-state resistance
 $R_{DS(on)} = f(T_j)$
 $I_D = -10A$; $V_{GS} = -10V$



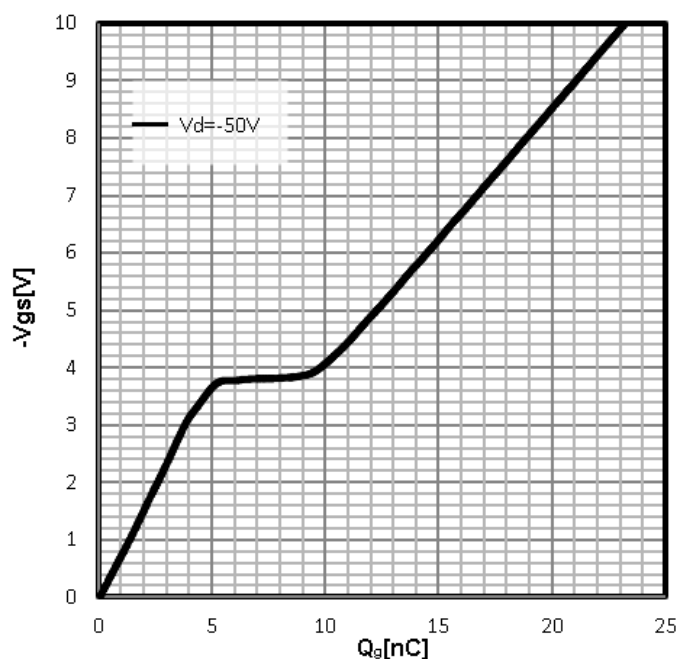
Gate Threshold Voltage
 $-V_{TH}=f(T_j)$;
 $I_D=-250\mu A$



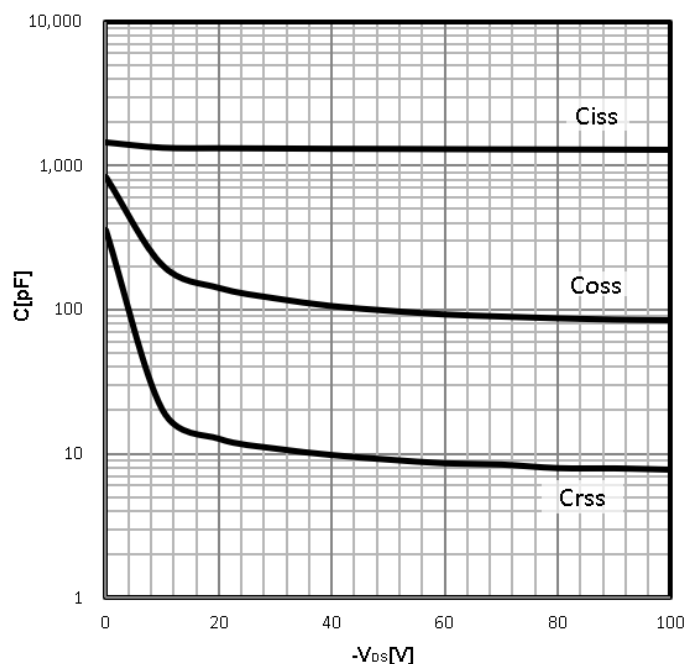
Drain-source breakdown voltage
 $-V_{BR(DSS)}=f(T_j)$; $I_D=-250\mu A$



Typ. gate charge
 $-V_{GS}=f(Q_g)$;
 $I_D=-10A$

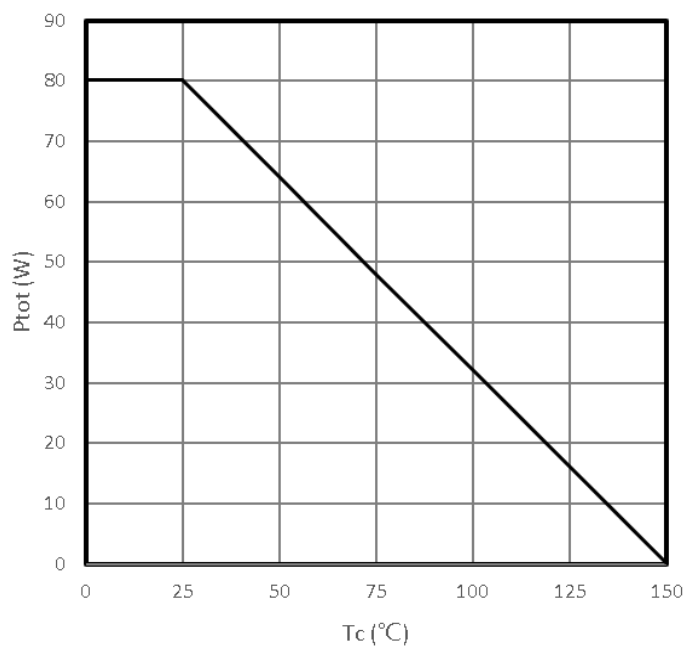


Typ. capacitances
 $C=f(-V_{DS})$; $V_{GS}=0V$; $f=1MHz$



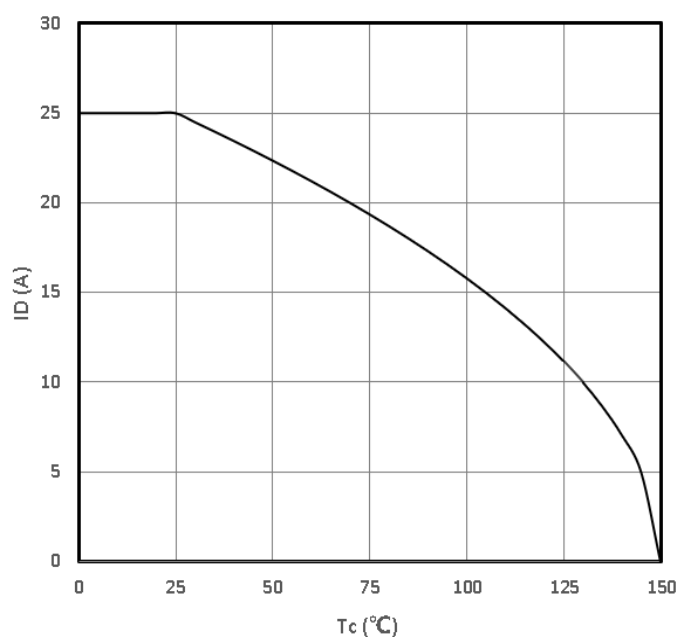
Power Dissipation

$$P_{tot}=f(T_C)$$



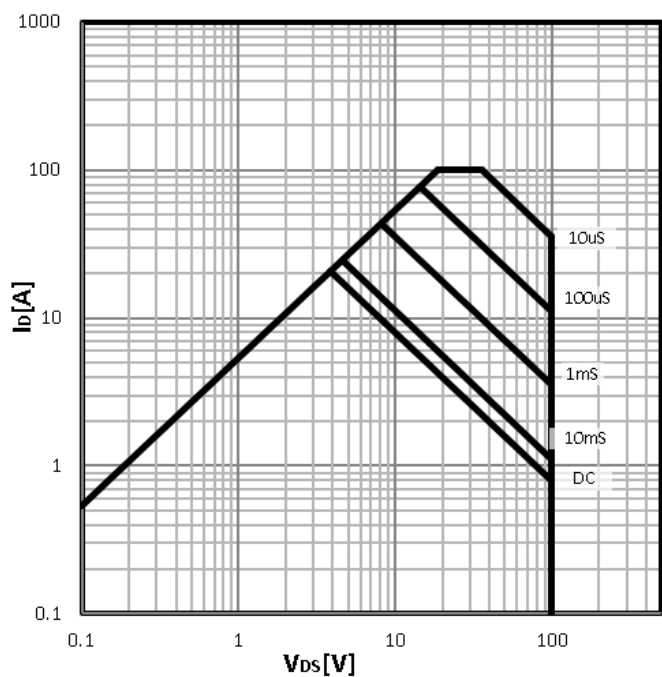
Maximum Drain Current

$$-I_D=f(T_C)$$



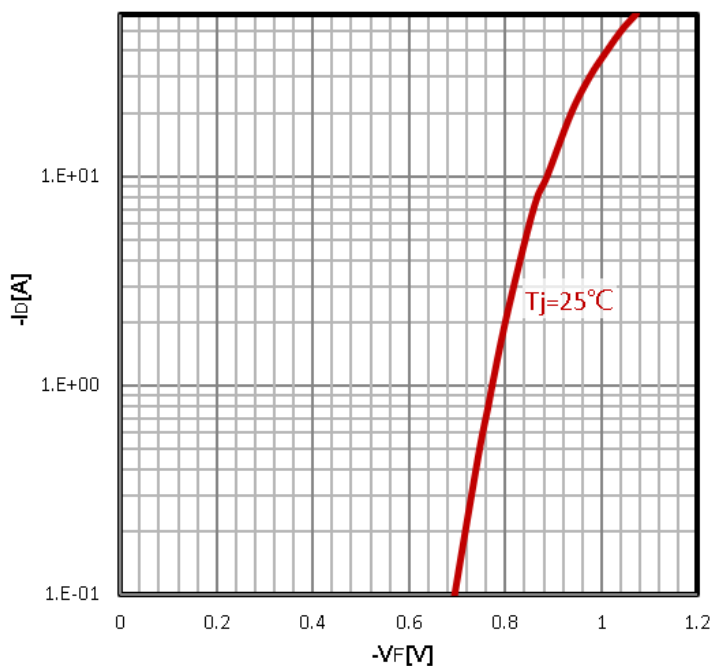
Safe operating area

$$-I_D=f(-V_{DS})$$



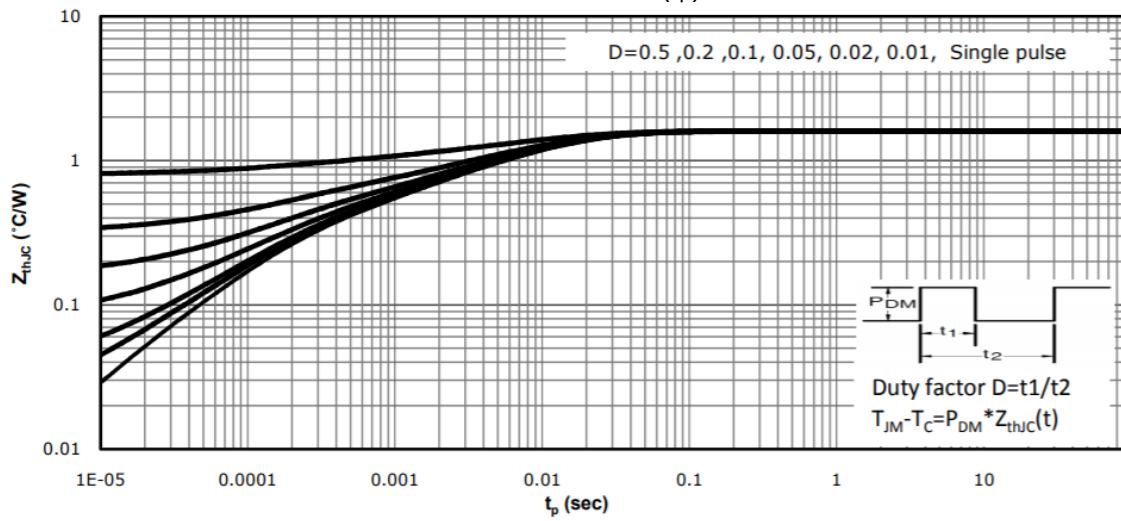
Body Diode Forward Voltage Variation

$$-I_F=f(-V_{DS})$$

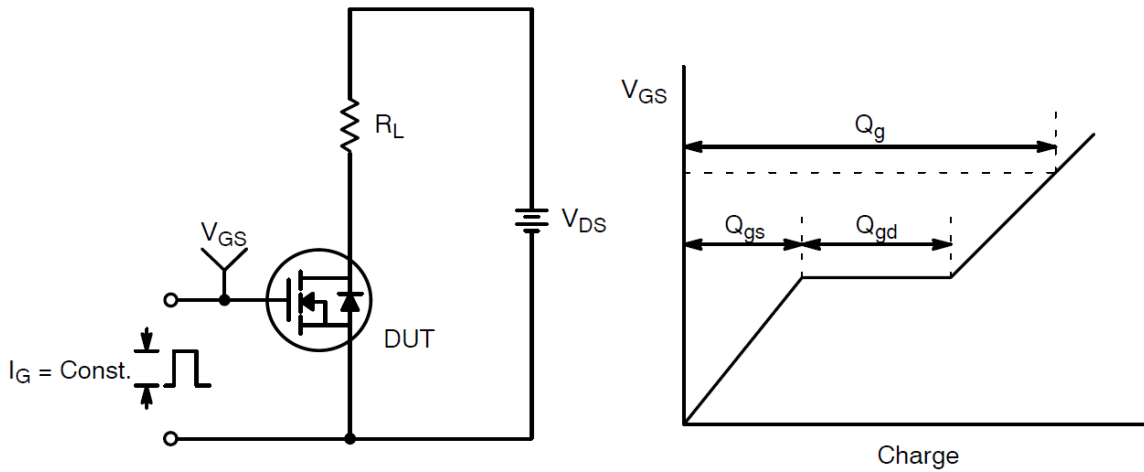


Max. transient thermal impedance

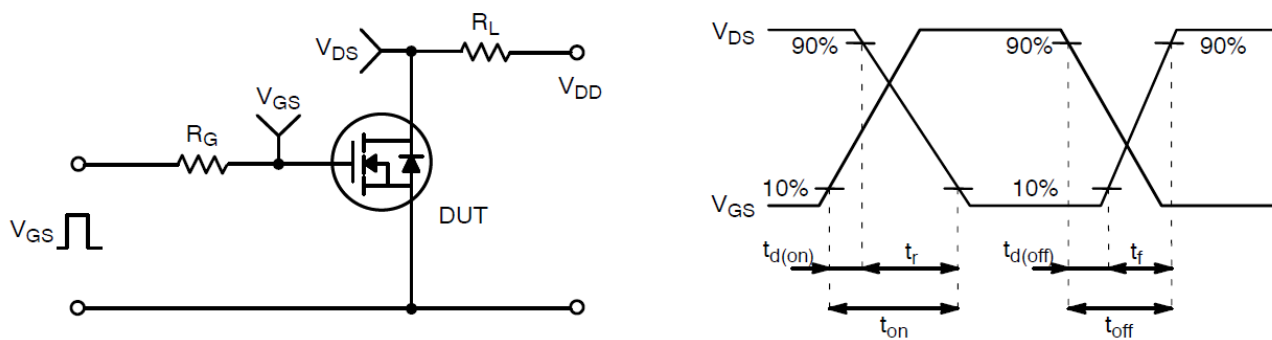
$$Z_{thJC}=f(t_p)$$



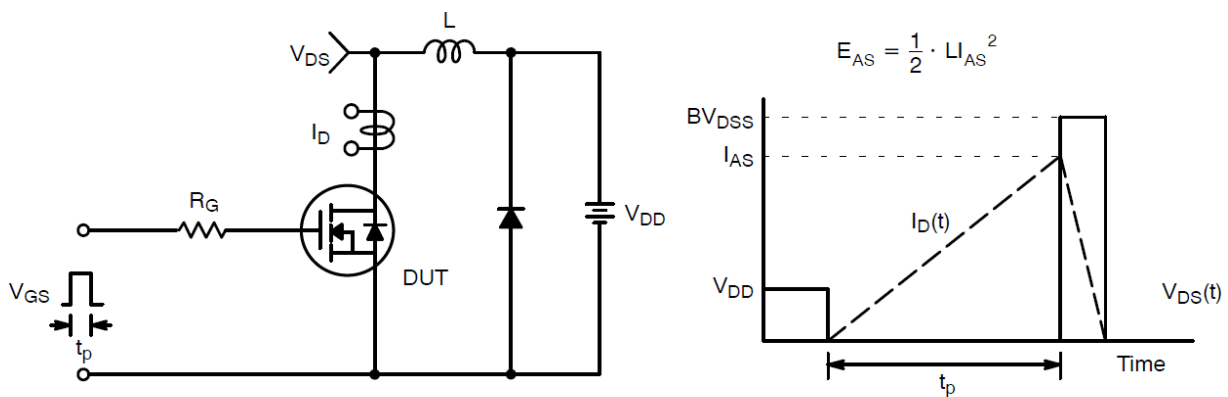
Test Circuit and Waveform:



Gate Charge Test Circuit & Waveform

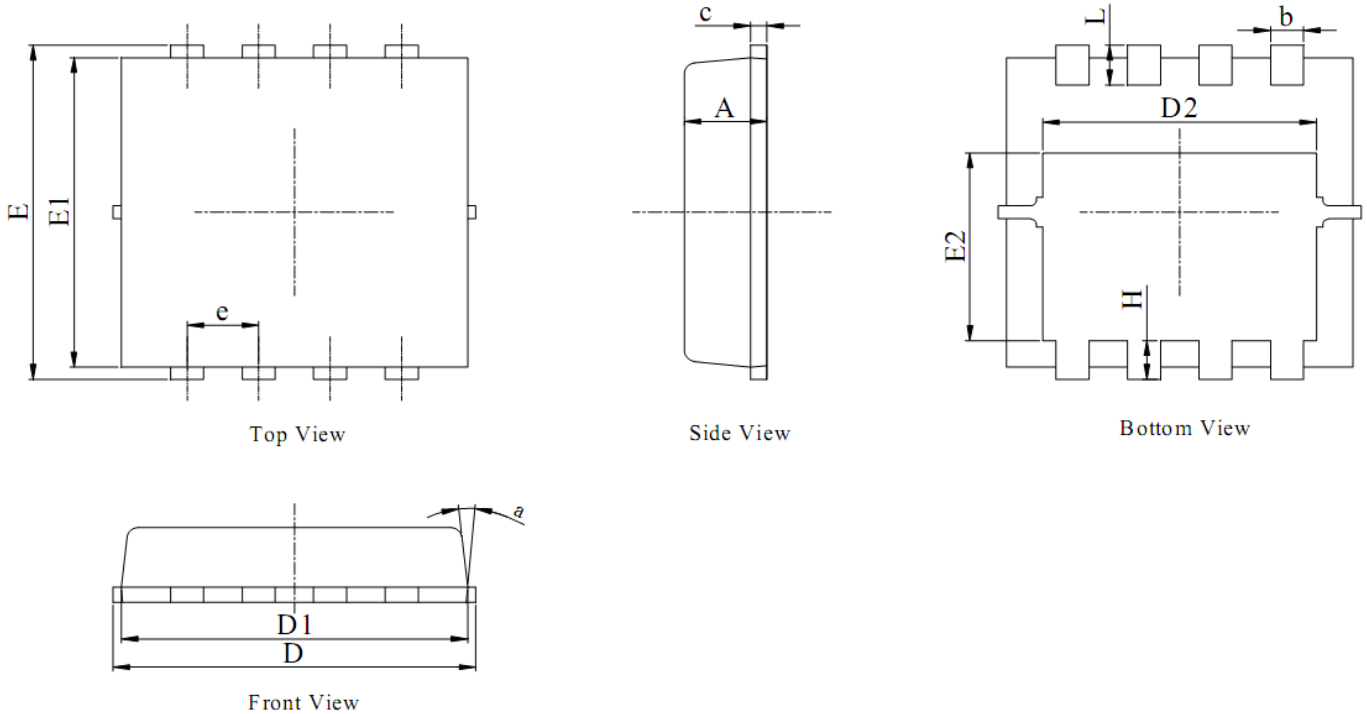


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

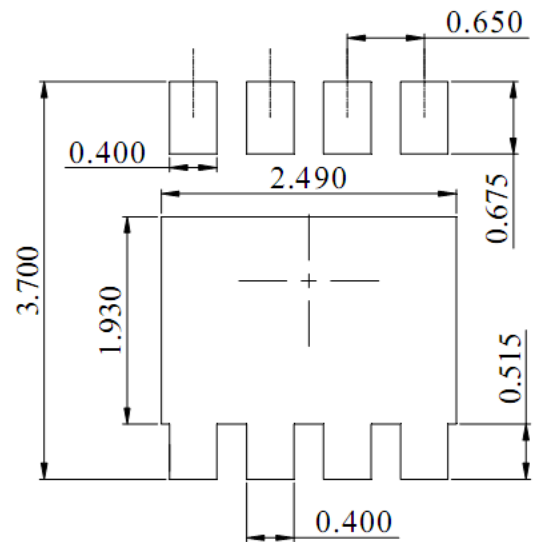
Package Mechanical Data-PDFN3333-8L-Single



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS